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Charge-Imaging Field-Effect Transistors for
Scanned Probe Microscopy

presented by

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Date May 7, 2001

Charge-Imaging Field-Effect Transistors for Scanned Probe Microscopy

A thesis presented

by

Lester Hao-Lin Chen

to

the Department of Physics

in partial fulfillment of the requirements
for the degree of
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in the subject of
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Charge-Imaging Field-Effect Transistors for Scanned Probe Microscopy

Robert M. Westervelt Lester Hao-Lin Chen

Abstract

This thesis presents experiments on integrating a charge-imaging field-effect transistor onto a scanned probe microscopy cantilever to make a moveable charge-imager. Such an imager would be used for imaging the spatial distribution of electric charge in semiconductor heterostructures and devices. Learning about the spatial distribution of charge yields knowledge about electrical transport at the microscopic level. The information gained from measuring the spatial distribution of charge increases with improvements in the spatial resolution and charge sensitivity of the charge-imaging probes. So, the goal is to devise a charge-imager with sub-micron spatial resolution and single-electron charge sensitivity.

To achieve high spatial resolution and excellent charge sensitivity, the charge-imaging field-effect transistors are made with a quantum point contact geometry. The charge response is confined to a disc with full width half-maximum comparable to its channel width, and the charge noise spectrum reaches values « 1 $e/Hz^{1/2}$ at 30 kHz. Their low power dissipation (< 10 μW) makes them suitable for operation at He dilution refrigerator temperatures.

A strain-sensing field-effect transistor integrated on the base of the same cantilever (*c.f.* Beck 1998a) allows for simultaneous topography-mapping. The strain-sensing field-effect transistor measures the strain caused by vertical deflections of the

cantilever to map the sample topography. The strain-sensing field-effect transistors have a white noise value for the deflection noise of 0.5 nm/$Hz^{1/2}$ at 10 kHz.

This thesis describes the fabrication and characterization of charge-imaging field-effect transistors and scanned microscopy cantilevers with integrated strain-sensing transistors. The transistors and cantilevers were fabricated in a GaAs/AlGaAs heterostructure using electron-beam lithography and were characterized at liquid Helium temperatures. Possible future experiments include demonstrating the charge-imaging FET's sensitivity to single electrons, creating a charge- and topography-imaging cantilever, and directly measuring the electron distributions in nanostructures.

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Chapter 1 Introduction

Section 1.1 Motivation

The more one sees, the more one knows.[1] To this end, the microscope has been an invaluable tool. Seeing cells with the optical microscope dramatically changed 18th century biological theories of living matter. However, Leeuwenhoek's invention is restricted to what can be seen with the human eye, and another tool was needed to discover if there was something smaller than the eye could see, *i.e.* atoms. The invention of the scanning tunneling microscope (STM) allowed imaging of individual atoms of conducting materials, and the atomic force microscope (AFM) (Binnig 1986) extended this capability to all materials. The AFM images a surface by scanning a cantilever across the surface and sensing the displacement the cantilever undergoes in response to forces from the surface. Images of individual carbon atoms have been acquired with an AFM using a cantilever with a self-contained displacement sensor (Tortonese 1993). The AFM has become a widely used tool (Rugar 1990), and it is used to measure many things besides the topography of a sample. This more general use of the AFM is called scanned probe microscopy (SPM), and magnetic forces, elastic properties, and capacitance can all be mapped with commercial SPM products (Howland 1996). The variety of SPM probes has not only increased knowledge but also advanced technology. One example is greater capacity in magnetic data storage. As the size of the storage devices has shrunk, an SPM probe sensitive to magnetic fields has become an invaluable diagnostic for verifying the proper functioning of the each successive generation of data storage devices.

[1] Philosophy students who disagree are invited to respond with their favorite epistemological argument.

Imaging the spatial distribution of electric charge in semiconductor heterostructures and devices yields knowledge about electrical transport at the microscopic level. To understand how electrical transport happens, it is necessary to see where the charge is. Measuring the electrical characteristics of a semiconductor device only gives information about the average movement of electrons. Moreover, details of electrical transport can be hidden by universal properties such as the resistance plateaus of a quantum Hall sample and the quantized conductance through a quantum point contact.

In a quantum Hall sample, transport theories have predicted "incompressible regions", edge states, and localized electrons. "Incompressible regions" are areas where charge does not accumulate, and edge states are areas at the sample edges where the current flows. The charge distribution of a two-dimensional electron gas (2DEG), a sheet of electrons free to move only in two directions, in the quantum Hall regime has been mapped with a sharp conducting SPM tip (Tessmer 1998). The tip is capacitively coupled to the 2DEG, and an ac excitation voltage in the 2DEG relative to the tip induces charge in the tip. However, charge is only induced in the tip when it lies over a regions of 2DEG, and areas with no response to the ac excitation voltage correspond to the predicted "incompressible regions". In a different experiment, the force on a metallic SPM tip caused by an ac excitation in the 2DEG relative to the tip was measured to image the voltage distribution in a quantum Hall conductor (McCormick 1999). These images show the currents at the sample edges, in agreement with theory. Finally, a single-electron transistor formed at the end of a glass tip over a 2DEG in the quantum

Hall regime has been used to image the structure of localized electronic states (Zhitenev 2000).

The quantum point contact (QPC) is another interesting system for study because the QPC current is composed of discrete modes. Quantum point contacts are often formed as narrow channels between electron reservoirs. A metal-coated SPM tip charged to a negative voltage relative to the 2DEG will deplete the 2DEG underneath. This creates a moveable scattering center underneath the tip. By measuring the conductance through the point contact as a function of tip position, the angular distribution of the current modes has been imaged (Topinka 2001a). Also, the current has been found to travel in branches (Topinka 2001b), a discovery which has led to theories about the structure of the potential through which the current travels and how the electrons interact with this potential. This builds on knowledge about the potential acquired using a scanning single-electron transistor probe (Yoo 1997).

The information gained from measuring the spatial distribution of charge increases with improvements in the spatial resolution and charge sensitivity of the charge-imaging probes. The utility of a probe is also related to the ease of its manufacture; knowledge only increases with widespread use. Thus, the goal is to devise a charge-imager with sub-micron spatial resolution, charge sensitivity capable of resolving single electrons, and ease of creation.

Section 1.2 Overview

Chapter 2 provides background on semiconductor heterostructures and devices. The devices are formed on a semiconductor material which contains a two-dimensional electron gas (2DEG), *i.e.* a sheet of electrons confined so they can only move in two directions. The first section describes how the semiconductor material is created to make a 2DEG. The two devices discussed are quantum point contacts (QPCs) and field-effect transistors (FETs), and their conductance characteristics will be described. Finally, the rationale for using cantilevers for scanned probe microscopy (SPM) is discussed. These cantilevers have integrated sensors for sensing deflection (Beck 1996) and charge.

Chapter 3 describes the experimental techniques used to fabricate and characterize our semiconductor devices and SPM cantilevers. An overview of the fabrication process and low-temperature electrical transport measurement techniques is given. For those interested in applying these techniques, Appendix A provides detailed descriptions of the procedures for operating the equipment used in fabrication of our semiconductor devices. Appendix C lists the companies that supply the necessary tools and equipment for both fabrication and measurements of our devices.

Chapter 4 discusses charge-imaging FETs that we designed and fabricated. These FETs have high spatial resolution and excellent charge sensitivity. These transistors can be integrated onto SPM cantilevers to make moveable charge sensors to directly image the spatial distribution of electric charge. The FETs have QPC geometries and the full width half-maximum of the spatial response was measured to be comparable to the FET channel width. The transistors have a charge noise level $q_n \ll 1\ e/Hz^{1/2}$ at 30 kHz.

Appendix B gives the computer programs used to analyze measurements of the FET characteristics.

Chapter 5 describes SPM cantilevers that we have fabricated with integrated strain-sensing and charge-imaging FETs. These cantilevers are designed for simultaneous charge-imaging and topography-mapping. The topography-mapping is achieved with the strain-sensing FET, which will detect any deflections of the cantilever (Beck 1998a). We measure the resonance frequency of the cantilever by mechanically exciting it and detecting the AC response in the drain current of the strain-sensing FET. We have also fabricated arrays of free-standing cantilevers, opening the possibility of using cantilevers in parallel to scan a larger area with greater speed.

Finally, Chapter 6 summarizes the experimental results of measurements of the charge-imaging FET and the SPM cantilevers. We review the spatial resolution and charge sensitivity of the charge-imaging FET and the mechanical response of the SPM cantilever. We also outline future experimental directions, including demonstrating the sensitivity of the charge-imaging FET to the charge of a single electron and fabricating arrays of charge-imaging and topography-mapping SPM cantilevers.

Chapter 2 Semiconductor Heterostructures and Electronic Devices

This chapter describes the physical properties of semiconductor heterostructures and electronic devices. Four topics are discussed: two-dimensional electron gases (2DEGs), quantum point contacts (QPCs), field-effect transistors (FETs), and scanned probe microscopy (SPM) cantilevers. Section 2.1 describes the formation and properties of a 2DEG. Section 2.2 gives the theoretical explanation of the quantized conductance through a QPC, its trademark signature. Section 2.3 describes the electrical properties of an FET, and Section 2.4 discusses the principles of using SPM cantilevers with integrated FETs for charge-imaging and strain-sensing.

Section 2.1 Two-Dimensional Electron Gases

A two-dimensional electron gas (2DEG) is a sheet of electrons quantum mechanically confined to two dimensions by a quantum well or accumulation layer in a $GaAs/Al_xGa_{1-x}As$ heterostructure. At low temperatures, the electrons do not have enough thermal energy to escape the lowest transverse state of the quantum well. Trapped in the ground state, the electrons are only free to move in the other two dimensions. Quantum wells and accumulation layers can be created by careful control of the thicknesses and compositions of the heterostructure layers. This control is achieved by using molecular beam epitaxy (Williams 1984, Maranowski 2000) to grow the heterostructure with atomic thickness resolution.

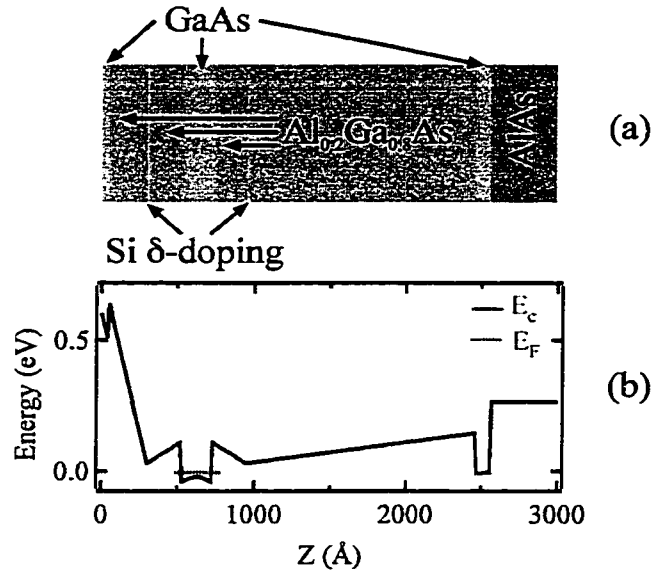

Figure 2.1 Layer composition and conduction band edge of the heterostructure denoted "Wafer 960220C". The heterostructure name is "Wafer YYMMDDA" where "YY" denotes the year, "MM" the month, "DD" the day, and "A" is a letter to order the heterostructures grown that day. The conduction band edge is plotted as a function of distance Z below the surface, and the dashed line indicates the Fermi level. Both diagrams have been drawn to the same length scale in the Z direction.

Figure 2.1 shows a heterostructure designed for the construction of free-standing cantilevers with integrated field-effect transistors (Beck 1996, 1998a). The light regions are GaAs layers, and the dark regions are $Al_xGa_{1-x}As$ layers. At a GaAs-to-$Al_xGa_{1-x}As$ boundary, there is a discontinuity in the conduction band edge $\Delta E_C(x)$ that depends on the Al mole fraction x

$$\Delta E_c(x) = 1.1x \text{ eV} \tag{2.1}$$

for $0 \leq x \leq 0.45$ (Blakemore 1987). This discontinuity forms the walls of the quantum well. Figure 2.1(b) plots the conduction band energy for the heterostructure shown in Fig. 2.1(a). In the 200 Å thick layer of GaAs that begins a depth Z = 520 Å below the surface, the conduction band edge is 0.22 eV lower than in the two $Al_{0.2}Ga_{0.8}As$ layers on

either side. The electrons for the 2DEG are provided by silicon dopant atoms of a carefully chosen sheet density. The dopant atoms create an electric field that creates a potential difference, as seen in Fig. 2.1(b) at Z = 300 Å. The doping density cannot be too high; otherwise, a parallel conduction layer is created. At the same time, the doping density must be high enough (typically 6 to 8×10^{12} cm^{-2}) to provide sufficient electrons to populate the quantum well.

The electrons in a two-dimensional electron gas (2DEG) can be confined by metal gates. Negatively charged metal gates deplete the 2DEG underneath, forcing current to flow in regions not depleted by the gates. A Schottky barrier between the metal and semiconductor allows the gates to be charged without conduction to the 2DEG. In equilibrium, bringing a metal and heterostructure into contact causes their Fermi levels line up. A large number of GaAs surface states pins the Fermi level 0.6 eV below the conduction band edge at the surface (Sze 1981), forming the Schottky barrier.

Section 2.2 Quantum Point Contacts

A quantum point contact (QPC) is a channel of width comparable to the wavelength of electrons that pass through it. A QPC connects two electron reservoirs, as shown in Fig. 2.2. A small applied voltage V raises the Fermi level of one reservoir slightly higher than the other by an energy eV. The electrons occupy subbands as they pass through the QPC, and narrowing the QPC width W decreases the number of subbands one by one below the Fermi level E_F. As a consequence, the conductance does not fall linearly as the width is decreased, but decreases in steps.

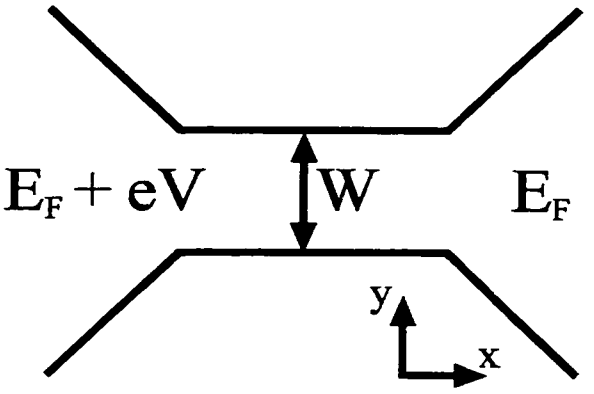

Figure 2.2 A schematic diagram of a quantum point contact of width W comparable to the Fermi wavelength. The quantum point contact connects two electron reservoirs with slightly different Fermi levels E_F and $E_F + eV$.

The current through the quantum point contact (QPC) is carried by electrons in subbands of the QPC. These subbands can be indexed, and the *n*th subband contributes a diffusion current:

$$I_{diff}^{n} = e\left(\int_{E_F}^{E_F+eV} \rho_n(E) v_n(E) dE\right) T_n \tag{2.2}$$

where $\rho_n(E)$, $v_n(E)$, and T_n are the is the density of states, group velocity, and transmission coefficient of the *n*th subband, and e is the electron charge. At T = 0 K, only electrons above the Fermi level contribute to the net current; so, the integral extends over the energy range $E_F \leq E \leq E_F + eV$. The density of states $\rho_n(E)$ and group velocity $v_n(E)$ can be expressed in terms of the dispersion relation $E_n(k)$ and the spin degeneracy g (Ashcroft 1976)

$$\rho_n(E) = g\left(2\pi \frac{dE_n(k)}{dk}\right)^{-1} \tag{2.3}$$

$$v_n(E) = \frac{1}{\hbar}\frac{dE_n(k)}{dk} \tag{2.4}$$

The dependence on the dispersion relation $E_n(k)$ cancels, and Eq. 2.2 simplifies to:

$$I_{diff}^n = e\left(\frac{geV}{h}\right)T_n \tag{2.5}$$

We obtain the QPC conductance G by applying the drift relation I = GV to Eq. 2.5 where I is the current, and V is the applied voltage (Beenakker 1991)

$$G = \frac{ge^2}{h}\sum_n T_n \tag{2.6}$$

If the electrons pass adiabatically through the quantum point contact (QPC), then each subband contributes equally to the current. The adiabatic condition implies the electrons do not change subbands as they pass through the QPC, and they are not partially reflected by the QPC. So, the transmission coefficients $T_n = 1$ for modes in the allowed energy range $E_F \leq E \leq E_F + eV$, and $T_n = 0$ for all others. The QPC conductance is $G = N(2e^2/h)$ where N is the number of energetically allowed subbands, and the spin degeneracy is g = 2. Thus, each time a new subband is added, the conductance jumps by $2e^2/h$ because the conductance of each subband is $2e^2/h$. So, the conductance increases in steps of $2e^2/h$ as the QPC width is increased.

Figure 2.3 illustrates a quantum point contact (QPC) formed in a 2DEG inside a heterostructure using electrostatic gates on the surface of the heterostructure. Ohmic contacts make electrical contact to the electron reservoirs to the left and right of the gates.

Electrostatic gates formed on the surface are negatively charged to deplete the 2DEG underneath. The gap between the two gates is 200 nm. When the 2DEG is depleted, a QPC of width W < 200 nm is formed in the 2DEG between the gates. The QPC width is electrostatically narrowed by making the gate voltage more negative.

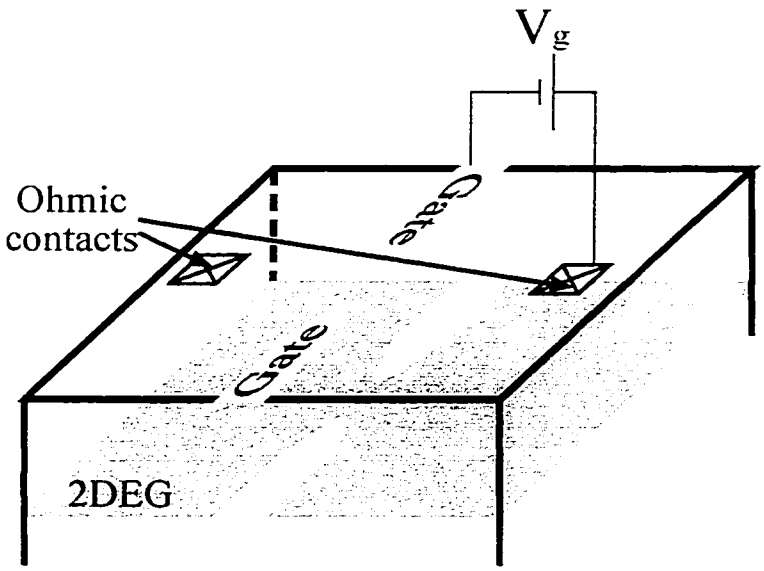

Figure 2.3 Schematic of a quantum point contact. Ohmic contacts make electrical contact to two-dimensional electron gas (2DEG) reservoirs to the left and right of the gates. To deplete the 2DEG underneath, the gates are charged to a negative voltage V_g relative to the 2DEG.

Figure 2.4 is a plot of quantum point contact conductance G vs. gate voltage V_g at T = 1.7 K. Conductance steps can be clearly seen, although they are not at exact multiples of $2e^2/h$ because of impurities and other scatterers.

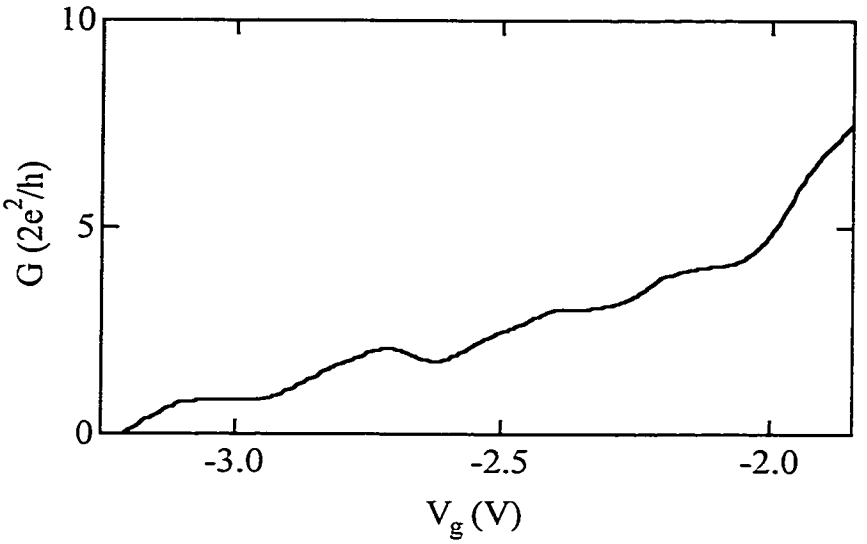

Figure 2.4 Quantum point contact conductance G as a function of gate voltage V_g at T = 1.7 K. The gate voltage is referenced relative to the source ohmic contact.

Section 2.3 Field-Effect Transistors

The section describes the electrical properties of field-effect transistors (FETs). Figure 2.5 shows an FET with channel length L and width W formed in a 2DEG by electrostatic gates and ohmic contacts on the surface of the heterostructure. It has drain and source contacts; voltage signals V_{GS} between the gate and source cause a change in the drain current. We will describe the FET drain characteristics – drain current I_D as a function of drain-to-source bias voltage V_{DS} for a series of gate-to-source voltages V_{GS} - and the noise spectrum. Considerations to minimize the FET noise level are also discussed.

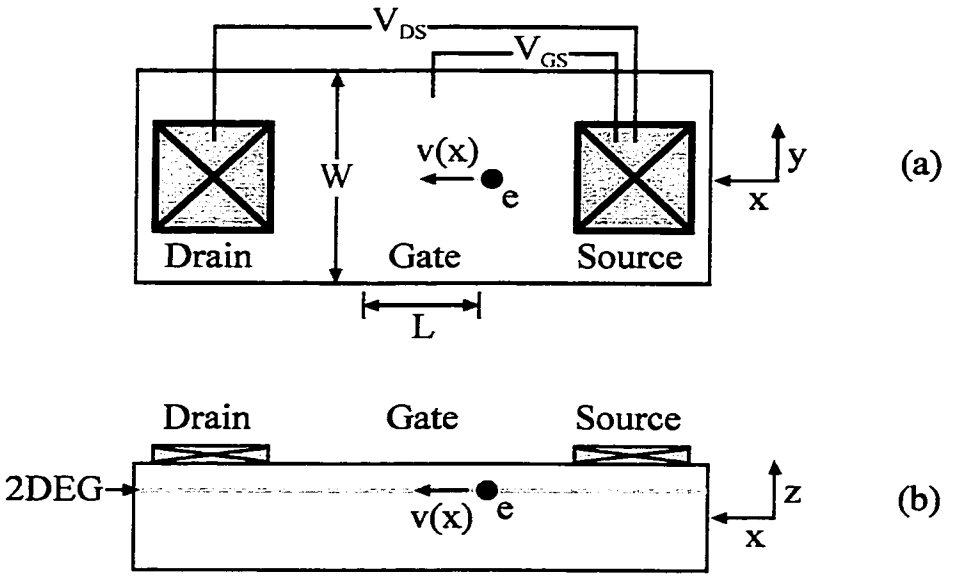

Figure 2.5 (a) Top view and (b) Side view of a field-effect transistor with channel length L and width W formed in a 2DEG. The drain is biased at a voltage V_{DS} relative to the source, causing electrons to flow from the source to the drain with a velocity v(x). The gate-to-source voltage V_{GS} controls the current flow.

First, we derive how the drain current I_D depends on the drain-to-source voltage V_{DS} and the gate-to-source voltage V_{GS} for an FET fabricated on a semiconductor heterostructure containing a two-dimension electron gas (2DEG). The drain current I_D can be expressed as (Delagebeaudeuf 1982)

$$I_D = eWn_s(x)v(x) \tag{2.7}$$

where $n_s(x)$ and $v(x)$ are the sheet density and electron velocity as a function of position x along the channel. Applying a gate-to-source voltage V_{GS} changes the sheet density of the 2DEG underneath the gate to

$$n_s(x) = \frac{\varepsilon}{ed}\left(V_{GS} - V_c(x) - V_{depl}\right) \tag{2.8}$$

where ε is the dielectric constant of the heterostructure, e is the electron charge, and d is the distance between the gate and the 2DEG. $V_c(x)$ is the voltage of the 2DEG relative to the source contact as a function of position along the channel, and V_{depl} is the gate-to-source voltage at which the 2DEG underneath the gate is depleted.

For small bias voltages, the FET acts as a resistor with resistance controlled by the gate voltage. The electron velocity is proportional to the electric field created by the bias voltage by the mobility μ.

$$v(x) = \mu \frac{dV_c(x)}{dx} \tag{2.9}$$

Applying Eqs. 2.8 and 2.9 to Eq. 2.7 yields the following expression for the drain current

$$I_D = \frac{\mu \varepsilon W}{d}\left(V_{GS} - V_c(x) - V_{depl}\right)\frac{dV_c(x)}{dx} \tag{2.10}$$

Integrating Eq. 2.10 over the channel length L yields a relationship between V_{DS} and the drain current I_D

$$\frac{V_{DS}}{I_D} = R_S + R_D + \frac{Ld}{\mu \varepsilon W\left(V_{GS} - V_{depl}\right)} \tag{2.11}$$

where R_S and R_D are the source and drain resistances.

For high drain-to-source voltages, the drain current saturates and is only weakly dependent on the drain-to-source voltage V_{DS}. The drain current saturates because the

bias voltage creates an electric field that pinches off the channel by depleting the 2DEG. The drain current has a saturation value

$$I_{sat} = \frac{\varepsilon W v_{sat}}{d}\left(\sqrt{(E_c L)^2 + \left(V_{GS} - V_{depl} - R_S I_{sat}\right)^2} - E_c L\right) \qquad (2.12)$$

The FET shown in Fig. 2.5 has a noise spectrum that decreases with frequency. This 1/f behavior[2] is caused by fluctuations in the number of electrons trapped underneath the gates (Duh in Savelli 1983). Similar noise spectra are found in metals and semiconductors. An 1/f spectrum can also be observed in a large variety of systems ranging from current noise in resistors to the frequency of flooding of the Nile River (Bell 1985).

The spatial sensitivity of an FET to external electric charge is increased by minimizing its channel area. The channel area can be made quite small ($< 0.1\ \mu m^2$) by making FETs with quantum point contact (QPC) geometries. The QPC geometry also minimizes the channel-to-gate capacitance C_{gc}, and this increases the FET roll-off frequency $f_{roll} = g_m/C_{gc}$ where the g_m is the transconductance, the change in drain current for a small-signal change in gate voltage about its bias point in the current-saturation regime.

Section 2.4 Cantilevers for Scanned Probe Microscopy

Figure 2.6 shows how a strain-sensing FET can be integrated onto the base of a scanned probe microscopy (SPM) cantilever (*c.f.* Beck 1996). The cantilever is a very

[2] Is broadly defined as fluctuations that behave as $1/f^{\alpha}$ where $0.8 < \alpha < 1.4$.

sensitive topography-imager (Beck 1998a) because the FET measures strain in the $\hat{e}_3$ direction caused by the vertical (along the $\hat{e}_1$ direction) deflections of the cantilever, as shown in Fig. 2.6(b). The dashed line is the line of no strain in the cantilever, and the arrows along the $\hat{e}_3$ direction indicate the strain of the cantilever. Above the line of no strain, the cantilever has expanded, and below it, the cantilever has compressed. In our cantilevers, $\hat{e}_1$ corresponds to [001], and $\hat{e}_3$ corresponds to [100].

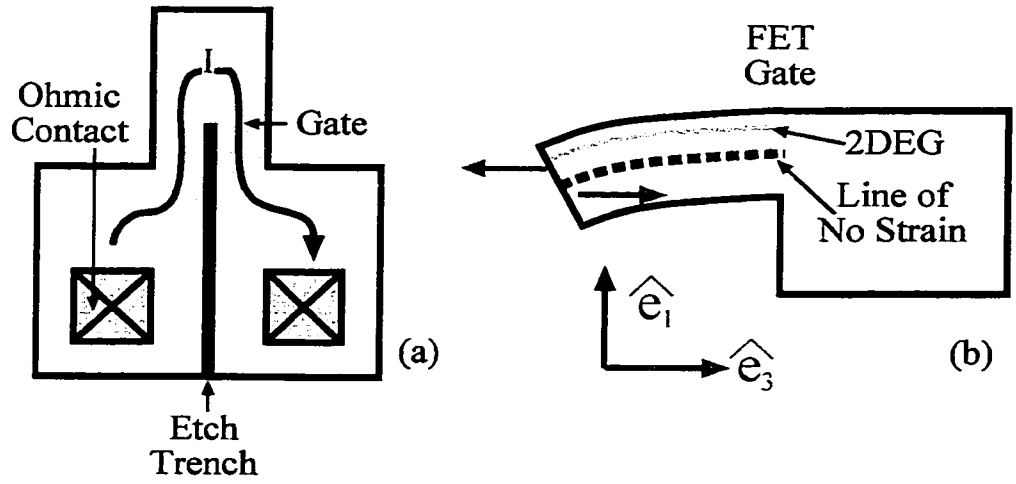

Figure 2.6 (a) Top view of a cantilever with an strain-sensing FET integrated at the base. The line indicates the current path created by the etch trench. (b) Side view of cantilever with directional axes indicated. The dashed line indicates the line of no strain in the cantilever, and the arrows indicate the direction of the strain. When the cantilever is deflected in the $\hat{e}_1$ direction, it is strained in the $\hat{e}_3$ direction.

Figure 2.7 illustrates how stress causes a polarization in the heterostructure. The polarization along the *i*-direction P_i is described in terms of the piezoelectric d_{ijk} and stress tensors σ_{jk} (stress along a the *j* -direction caused by a strain in the *k*-direction) (Fricke 1991)

$$P_i = \sum_{j,k} d_{ijk}\sigma_{jk} \tag{2.13}$$

In the cantilever shown in Fig. 2.6, the deflection along $\hat{e}_1$ causes a strain along $\hat{e}_3$, and thus a stress along $\hat{e}_3$. This results in a polarization along $\hat{e}_1$ of $P_1 = d_{133}\,\sigma_{33}$ where $d_{133} = -2.69 - 1.13x$ pC/N (Blakemore 1987) is the relevant element in the piezoelectric tensor of $Al_xGa_{1-x}As$. The amount of strain is different for each heterostructure layer; so, the polarization will vary from layer to layer. The difference in the polarization of two adjacent layers causes surface charge to build up at the layer boundaries. This surface charge changes the FET drain current, which can be measured to determine the cantilever deflection.

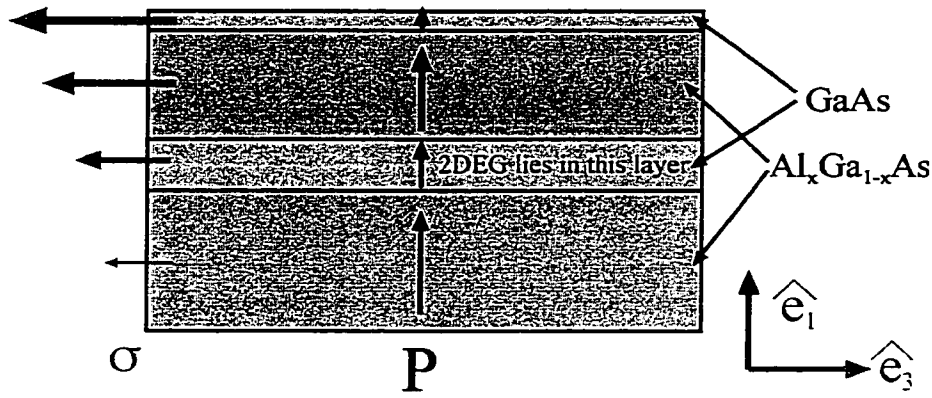

Figure 2.7 Strain along the $\hat{e}_3$ direction causes a stress σ, which varies linearly from layer to layer, as shown by the arrows pointing along $\hat{e}_3$. The length of the arrows indicates the amount of stress. The stress results in a polarization P, which is shown by the arrows in the $\hat{e}_1$ direction. The polarization varies from layer to layer due to the varying stress and the different piezoelectric constants of the layers of the $GaAs/Al_xGa_{1-x}As$ heterostructure.

As will be discussed in Chapters 4 and 5, adding a second, charge-sensing FET onto the tip of the scanned probe microscopy (SPM) cantilever shown in Fig. 2.6 would make a moveable charge imager. This charge-imaging SPM cantilever can be used to image the electron flow through semiconductor nanostructures. The thermal energy of the cantilever causes a vertical deflection of $z_T = 1.3$ Å ($T = 300$ K) which is much less than the height (~ 10 nm) of the nanostructure features. The thermal deflection z_T, is

calculated by equating the thermal energy 1/2 k_BT of the cantilever with its potential energy 1/2 $k_{cant}z_T^2$, where k_{cant} is the cantilever spring constant. For small deflections, the spring constant is (Feynman 1964)

$$k_{cant} = \frac{3EI}{L^3} \tag{2.14}$$

$$I = \tfrac{1}{12} wh^3 \tag{2.15}$$

for a cantilever of length L, width w, thickness h, and Young's modulus E. The quantity I is the rotational moment of the cantilever for vertical deflections. The cantilevers described in Chapter 5 have length L = 35 μm, width w = 20μm, thickness h = 0.255 μm, and Young's modulus E = 119 GN/m^2 (Blakemore 1987). They have a spring constant of k_{cant} = 0.23 N/m, which was used to calculate the thermal deflection z_T.

The nanostructure topography can be measured without touching the cantilever to the nanostructure. Forces from the sample, *e.g.* van der Waals forces, alter the spring constant of the cantilever. The cantilever's intrinsic resonant frequency f_{res} is directly related to its spring constant k_{cant} (Chen 1993)

$$f_{res} = \sqrt{0.31 \frac{k_{cant}}{M}} \tag{2.16}$$

where M = ρLwh is the mass of a cantilever of density ρ, length L, width w, and thickness h. Thus, a cantilever mechanically excited at its resonant frequency will be pushed off resonance by a nearby surface.

Chapter 3 Experimental Techniques

This chapter describes the storage and handling of semiconductor heterostructures, device fabrication, and performing low-temperature measurements. No experiment can be performed without the proper tools; so, throughout the chapter, the tool and equipment companies are referenced using the notation "(ABC – Item # ___)". "ABC" is the three-letter company code from Appendix C, and "Item # ___" is the item number used for ordering.

Section 3.1 $GaAs/Al_xGa_{1-x}As$ Heterostructures

The heterostructure material must be carefully stored and handled to preserve its electrical properties. Oxidization, surface damage, and electrostatic damage are the most common threats to the two-dimensional electron gas (2DEG) in the heterostructure; so, the techniques described in this section will focus on these three. Oxidization can change the electrical properties and physically damage the heterostructure. Surface damage almost always destroys the 2DEG because the 2DEG lies only 52 nm below the surface.[3] Electrostatic damage is when an extremely high electric field causes dielectric breakdown of the heterostructure and destroys the 2DEG. These high electric fields arise between the gates and the 2DEG, which are separated by only 52 nm. A small voltage (0.5 V) between them yields a substantial electric field of 10^7 V/m.

To prevent oxidization, the heterostructure wafers are stored in a "nitrogen dry-box". Nitrogen gas continually flows through the "dry-box" to maintain a pressure above atmosphere and prevent oxygen in the air from entering. The nitrogen gas is obtained

[3] For comparison, the scribe marks made during cleaving are tens of micrometers deep.

from the boil-off of a liquid nitrogen storage dewar; so, the gas is free from water vapor or other sources of oxygen. Samples should be processed quickly once they have been cleaved from the wafer.[4]

To avoid scratching the heterostructure surface, it is best to use Teflon tweezers (FWI – Item #C10-05A02). Using metal tweezers with even moderate forces can often create deep (~ 100 μm), seashell-shaped divots on the sides of the sample. Not only do these divots remove the 2DEG and potentially large portions of the device, but they also weaken the structural integrity of the sample. Extra care should be taken when using metal tweezers is unavoidable, *e.g.* transferring a sample to a hot plate.

To prevent electrostatic damage to the samples, they should be stored in anti-static containers (FWI – Item # H20-426-62C02, H20-02-62C02) and handled with anti-static tweezers. The containers and tweezers are made of a polypropylene which contains carbon powder. This material exponentially dissipates any built-up voltage with a time constant < 0.01 s. Any metallic tools, *e.g.* scalpel, should be electrically connected to earth ground during use. Finally, wearing a grounding strap whenever possible is good practice.[5]

[4] For absences over a week, *e.g.* winter recess, it is best to put samples back in the "dry-box" for the duration.

[5] As is taking off wool or Polartec garments to prevent the handler from becoming the destroyer.

Section 3.2 Device Fabrication

This section describes all possible steps in fabricating a device on a $GaAs/Al_xGa_{1-x}As$ heterostructure. The general principles of each step are discussed, but the step-by-step procedures for operating the equipment are described in Appendix A. All devices described in this thesis can be fabricated using the above processes; some were made using only a subset.

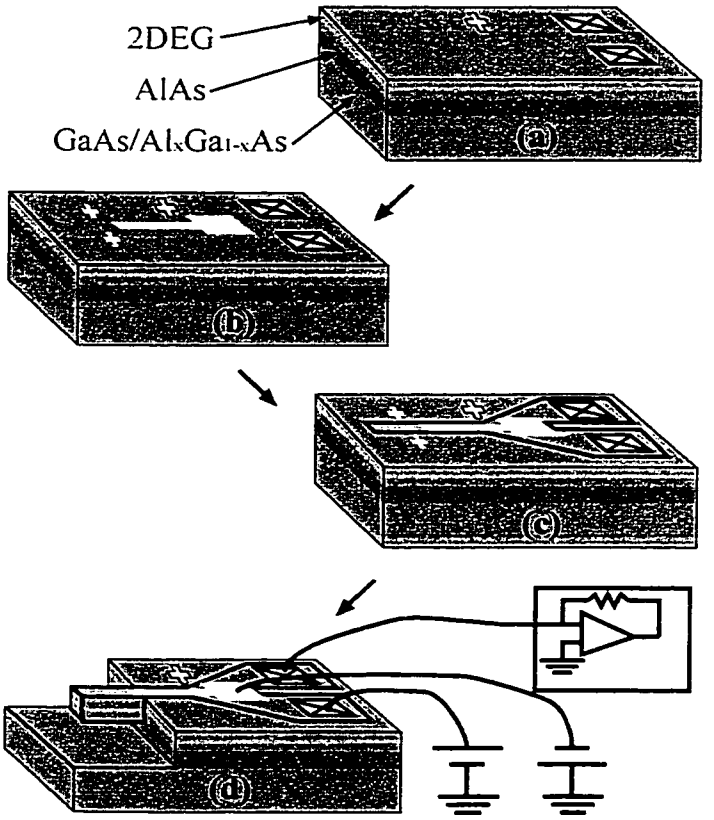

Figure 3.1 Overview of the device fabrication process. (a) Ni:Au:Ge ohmic contacts and the alignment markers to be used at magnification 20× are thermally deposited and annealed. (b) Cr:Au electrostatic gates and magnification 200× and 1000× alignment markers are thermally deposited. (c) Etch trenches (black lines) are formed by ion milling. (d) Hydrofluoric acid etching the AlAs layer to form a free-standing cantilever, and then wirebonding leads to the ohmic contact and gate pads.

Subsection 3.2.1 Device Design

The first step is drawing the device using the DesignCad drafting program. The DesignCad file is used by the Nanometer Pattern Generation System (NPGS) program to control the electron beam during lithography. The specific device, *e.g.* a quantum point contact, depends on the experiment, but there are some general design guidelines:

1. Sections to be written at different magnifications must overlap to insure continuity. An overlap of 0.5 % of the larger field of view (80 mm/magnification value) is sufficient. For example, sections written at magnifications 20× and 200× should overlap by $0.005 \times (80\ \text{mm}/20) = 20\ \mu\text{m}$.
2. The ohmic contact and gate pads should be placed far (> 600 μm) from the active region of a device. This is so the Au wires wirebonded to the pads do not interfere with an external probe, *e.g.* scanned probe microscopy cantilever.
3. Alignment markers should be formed in pairs so the NPGS alignment program can calculate a rotation matrix from the relative positions of the two markers. It is preferable to have two pairs in case one set is either not properly formed or destroyed.
4. Alignment markers should be located so if a square enclosing them is destroyed, then the device is not affected.

The DesignCad program draws devices as a series of filled polygons. The polygons can be placed in different layers and colors, which correspond to different magnifications and electron beam dosages, respectively. The NPGS manual (Nabity 1997) describes the details of using the DesignCad program for lithography, but the most commonly used commands are listed below:

1. To create a filled polygon, press "ALT-F5". Then press the ":" key and enter the vertex coordinates. Repeat the second step until all vertices have been specified.
2. The "CHANGE" command on the "EDIT" menu allows the user to alter the color and layer of a polygon.
3. "L" allows the user to select which layers are displayed.
4. The right-hand mouse button snaps the cursor to the nearest vertex.
5. "Z" sets the zoom.

A separate DesignCad file must be made for aligning the electron-beam lithography steps. This alignment file uses scan windows and overlays to describe the alignment marker locations. A scan window is an area over which the electron beam is swept and the measured detector response displayed as an image on the computer screen. An overlay is an outline of where an alignment marker should be. Both scan windows and overlays are drawn as filled polygons, but they have different "LINE TYPE"s: "1" for scan windows and "0" for overlays.

After the DesignCad files have been made, the parameters for each layer must be specified in a "run file". The parameters are: magnification, origin offset, center-to-center and line spacings, and beam dosage. The "run file" is created by entering the command "mrf device (align)" where "device.dc2 (align.dc2)" is the the device (alignment) DesignCad file.

The magnifications used for the devices in this thesis are 20×, 200×, and 1000×. When performing lithography, one begins at a high magnification and zooms out to lower magnifications. When performing alignment, one begins at low magnifications and zooms in to high magnifications.

The origin offset is used to line up the origins of different magnification-beam current combinations. The origin positions can be measured from the lithography pattern shown in Fig. 3.2. The Olympus BH2-UMA optical microscope at magnification 500× has calibrated markings that can be used to measure the distance between the features in Fig. 3.2. Comparing the measured distance with the distances in the DesignCad file yields the origin offsets.

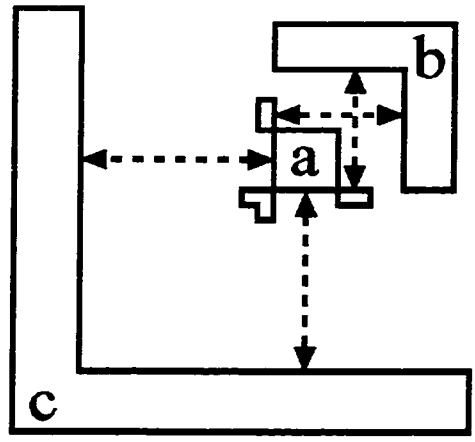

Figure 3.2 Lithography pattern used to measure the origin offsets. The areas drawn with solid lines were patterned at magnification (a) 1000× (b) 200× (c) 20×. The dashed lines indicate the distances to be measured to determine the origin offsets.

The center-to-center and line spacings are the distances between consecutive points and consecutive lines in the series of dots that make up a filled polygon. Figure 3.3 illustrates the two spacings. During lithography, these spacings determine the spot density, and during alignment, they set the pixel size of the image that is obtained from measuring the detector response while sweeping the electron beam over the scan window. Table 3.1 lists typical values for the two spacings, which are usually set equal to each other. Alignment between lithography steps is guaranteed to within twice the (center-to-center) spacing, but with practice, one can achieve accuracy equal to the spacing.

The beam dosage specifies the charge density the pattern is exposed to during lithography. To determine the optimal value (300 to 550 $\mu C/cm^2$), lithography of a pattern is repeated for a series of different dosage values. The series of patterns is examined to determine which dosage value yielded the sharpest features. The beam dosage values are used only in the device "run file". The beam dosage values in the alignment "run file" are ignored by the alignment program.

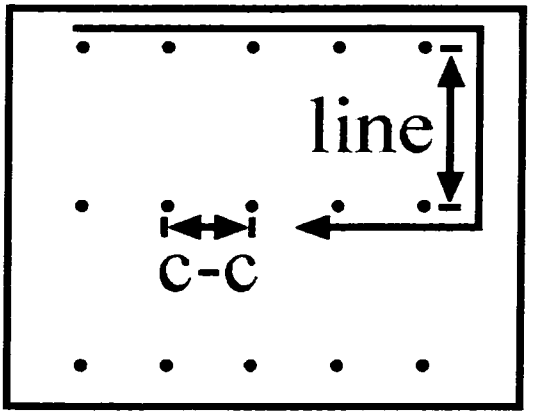

Figure 3.3 The pattern of dots used to fill a polygon during electron-beam lithography. The dots are drawn in the order indicated by the solid line. The distance labeled "c-c" is the center-to-center spacing. The distance labeled "line" is the line spacing.

Magnification	20×	200×	1000×
Device	6700 Å	1000 Å	67 Å
Alignment	20000 Å	8000 Å	500 – 1500 Å

Table 3.1 Center-to-center and line spacings.

Subsection 3.2.2 Cleaving

Cleaving (Appendix A.1) creates millimeter-sized chips from 3 inch-diameter heterostructure wafers. This subsection discusses how to choose the size of the chips and reviews the cleaving process.

A chip with side length of 2 to 3 mm usually has sufficient area for any device. This size is still small enough that a large number of chips can be cleaved from the heterostucture wafer. The chip size is determined by how much area is needed to fit the device, including leads and bonding pads. The number of bonding pads tends to dictate the chip size as the pads have large areas ($\geq 200 \times 200\ \mu m^2$) and are well separated from each other ($\sim 100\ \mu m$). A 100 μm wide border around the device protects the device from rough handling.

Cleaving is causing the heterostructure wafer to break along a desired line. The line is defined by scribing[6] with a diamond-tipped pencil. The wafer is laid over a microscope slide covered with Teflon tape, with the scribed line directly above the slide edge. The wafer is held to the slide by pressing gently on it with a folded circle of filter paper[7]. Another piece of folded filter paper is pressed on the overhanging portion until the heterostructure breaks along the scribed line. Both pieces are cleaned of GaAs dust by spraying with methanol (D&I – Item #M-371-008) and blow-drying with ultra-high purity nitrogen (UHP) gas (IGO).

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[6] Previous theses (Katine 1996) have described only scribing a small segment of the cleave line desired. While this technique does lead to straighter, cleaner cleaves, it carries a higher risk of a cleave occurring along a line not defined by the scribes.

[7] Filter paper will not scratch the surface.

Subsection 3.2.3 Electron-Beam Lithography

Electron-beam lithography uses a scanning electron microscope (SEM) to pattern polymethylmethacrylate (PMMA) resist on a chip. The process consists of three steps: applying as PMMA negative resist (Appendix A.2), exposing a pattern in the resist using the JEOL SEM (Appendix A.3), and washing away the exposed resist.

The PMMA resist should be spun onto clean chips so the PMMA adheres well and no dust particles mar the resist surface. The chips are placed in small Teflon beakers and cleaned with a series of semiconductor-grade organic solvents. The chips are boiled in trichloroethylene (D&I – Item #3–9454) and then sonicated in acetone (D&I – Item #A-176-008). Still immersed in acetone, the chips are taken to the inner (Class[8] 100) cleanroom and sonicated in methanol. After being blown dry with nitrogen gas, the chips are placed in covered anti-static containers. Then, the PMMA resist is applied by pipetting a drop of PMMA dissolved in anisole onto the chips. The chips are immediately spun (Appendix A.2) at high speed (3 to 5 krpm) and baked on a hot plate at T = 180 °C. Additional layers of resist are applied after the chip has been baked dry.

The chips are affixed to sample mounts with carbon paint to prepare them for lithography (Appendix A.3). Each chip must be mounted flat so a good focus can be maintained across the chip area. Therefore, care should be taken that carbon paint does not get underneath the chip. Also, it is best to mount one chip per sample mount, as there is often not a sufficiently large, clean area to mount a second chip. Flecks of silver paint are left on the PMMA surface to provide high-contrast objects for focusing the scanning

[8] Class N meas there are less than N particles of size greater than 0.5 micrometers in diameter in a cubic foot of volume.

electron microscope at high magnifications (100,000×). The silver paint flecks are left ~ 100 μm in from the chip corners so the thicker PMMA at the chip edges does not put them on a different focus plane from the center of the chip. In addition, focusing at the corners will not expose the chip center, where the fine device features are usually located.

The main steps of performing lithography with the JEOL scanning electron microscope (SEM) are listed below:

1. Raise the stage so the chip is a working distance 15 mm below the SEM filament.
2. With the chip out of the field of view, turn up the SEM filament current until it saturates.
3. Adjust the SHIFT (center position of beam) and TILT (angle of beam) settings to obtain the maximal, stable SEM current.
4. Adjust the stage and scan rotations so the edges of the chip are vertical and horizontal on the screen.
5. Focus on the silver paint flecks and enter the average of the focus settings into the SEM control program.
6. Adjust the beam stigmation so the beam has a circular cross-section.
7. Measure the beam current at the condenser lens values to be used.
8. Use the Nanometer Pattern Generation System (NPGS) alignment program to align the chip.
9. Use the NPGS pattern generation program to pattern the resist.
10. Shut down the SEM beam and remove the sample mount from the SEM chamber.

The pattern is formed by washing away the PMMA resist that has been exposed to the electron beam. This process is called "developing" because the pattern appears in the PMMA much as a photograph appears after the print is placed in developer solution.

1. Gently push the edge of a clean scalpel blade between the bottom of the chip and the top of the sample mount. Use the minimal amount of force necessary to free the chip.
2. With anti-static tweezers, remove the chip from the sample mount and place it in an anti-static container.
3. Fill a small petri dish with enough developer solution (6.5 ml methyl ethyl ketone (MEK) : 125 ml 4-methyl-2-pentanone (MIBK) : 375 ml isopropyl alcohol (IPA)) to cover the chip.
4. Place the chip in the developer solution and gently agitate the petri dish so the solution washes back and forth over the chip for 30 s.
5. Spray the chip with IPA (D&I – Item #I-341-008) for 10 s.
6. Blow the chip dry with ultra-high purity nitrogen gas, taking care to blow the tweezers dry too.
7. Examine the chip with an optical microscope. PMMA that was exposed to the electron beam should be gone, and a pattern of PMMA-free GaAs should be clearly seen.

The pattern will be improperly formed if either too low or too high an electron beam dosage was used during lithography. The beam dosage is insufficient if some portions of the pattern appear filled with islands of PMMA. It may be possible to remove these islands by repeating Steps 4-6. If two repetitions are not sufficient, then the pattern must be redone. The beam dosage is excessive if the pattern boundaries appear blurred.

If the blurring is tolerable, then simply use a smaller beam dosage for the next sample. If the blurring is too much, then the pattern must be redone. To redo the pattern, soak the chips in acetone for an hour to remove the PMMA, apply new PMMA, and repeat the lithography with an adjusted beam dosage.

Subsection 3.2.4 Ohmic Contacts

Ni:Au:Ge ohmic contacts make electrical contact to the two-dimensional electron gas (2DEG). Ohmic contacts are formed using electron-beam lithography, thermal deposition of Ni, Au, and Ge (Appendix A.4), the lift-off technique, and annealing. Figure 3.4 illustrates the first three steps. The contacts are patterned in a trilayer of PMMA resist to minimize the number of pinholes in the resist. These pinholes must be avoided as they allow formation of miniature, unwanted ohmic contacts that electrically short any metal gates that cover them to the 2DEG.

The magnification 20× alignment markers are also formed at the same time because the ohmic contacts are the first features to be fabricated. This allows later lithography steps to be aligned to the contacts. The magnification 200× and 1000× alignment markers are formed later because annealing distorts the shape of the markers, affecting the accuracy of alignment at high magnifications.

The Ni, Au, and Ge are deposited by thermal evaporation after the PMMA resist has been patterned using electron-beam lithography. The chips are mounted with carbon paint onto a copper[9] evaporation stage. The stage is loaded into a thermal evaporator and clamped to an air-cooled platform. A thermal evaporator consists of a power supply with

electrical feedthroughs inside a large bell jar which is evacuated to a medium vacuum (0.5 μT). Tungsten boats (RDM – Item # S47-020W for Ni, #S9A–010W for Ge, Au) connected to the feedthroughs complete an electric circuit with the power supply. Four 1/4"-length pieces of Ni wire (AAI – Item #10929) are placed in the first boat, one 0.1 cm^3 piece of Ge (AAI – Item #10191) is placed in the second boat, and about twelve 1 mm^3 pieces of Au (cut from a Canadian maple leaf coin) are placed in the third boat. The boats are heated by Joule heat from the power supply until the metals they hold melt and evaporate. Above the boats, the stage is covered with an Al-foil shutter, which is opened and closed to allow the desired amount of evaporated metal to coat the chips. The thickness of deposited metal is measured using a crystal monitor. For ohmic contacts, the following sequence of metals is evaporated: 50 Å Ni, 50 Å Au, 250 Å Ge, 450 Å Au, 100 Å Ni, and 400 Å Au. The chips are let to cool before being unloaded from the evaporator.

The unwanted metal is removed using the lift-off technique. The chips are unmounted from the stage and placed in acetone for ~ 1 hour to dissolve the PMMA. This lifts off the metal that lay on it, leaving only metal that was deposited on the GaAs surface. If lift-off is not complete after an hour, an overnight soak in acetone is recommended. If lift-off is still difficult, then sonication for brief (< 1 s) periods may be used. Once lift-off is complete, the chip is blown dry using ultra-high purity nitrogen gas.

Annealing (Section A.5) diffuses the Ni:Au:Ge below the surface to make electrical contact with the two-dimensional electron gas. The chips are annealed on a

[9] Copper is used for good thermal conduction to an air-cooled platform, but the chips are mounted on an aluminum plate epoxied to the stage to prevent the copper from diffusing into the chips.

Joule heated tungsten strip inside a chamber filled with forming gas (IGO - 80% helium, 20% hydrogen). The temperature of the tungsten strip is measured with a thermocouple soldered to the underside of the tungsten strip. The chips are heated to 110 °C to boil off moisture, then to 250 °C to prime it, and finally to 410 °C to anneal. To insure the chip is evenly annealed, the annealing process is repeated with the chip rotated 180°.

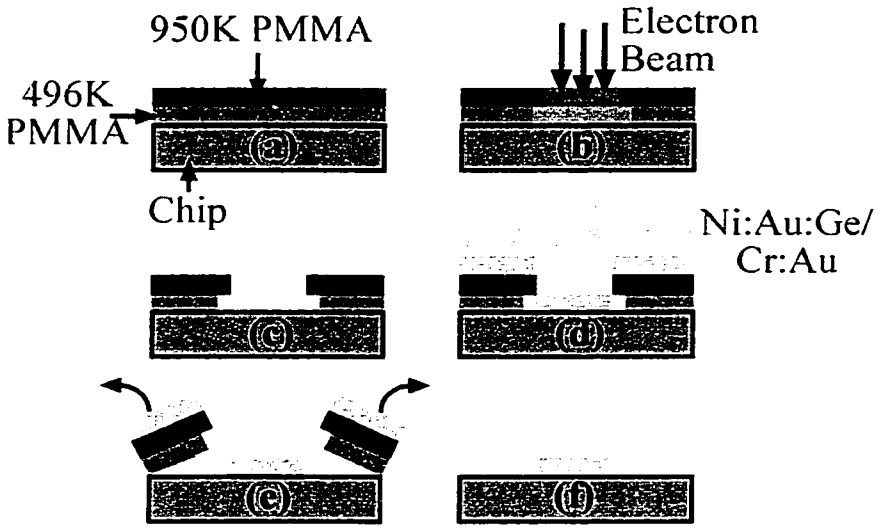

Figure 3.4 Metal deposition and lift-off process. (a) Spin PMMA resist. (b) Perform electron-beam lithography of the desired pattern. (c) Develop the PMMA. (d) Thermally evaporate metal. (e) Lift-off undesired metal. (f) Only metal in desired pattern remains.

Subsection 3.2.5 Electrostatic Gates

Cr:Au gates are used to electrostatically deplete the two-dimensional electron gas (2DEG) underneath them. Cr:Au gates formed using electron-beam lithography (Appendix A.3), thermal deposition (Appendix A.6), and the lift-off technique, as shown in Fig. 3.4. Lithography is performed on a bilayer of resist because there is no danger of the gate metals shorting to the 2DEG. Chromium is evaporated first to wet the GaAs surface and to aid adhesion of the Au layer. The gold prevents the gates from oxidizing

and keeps the resistance low. The gates are not annealed; so, very sharp features can be formed. For this reason, the magnification 200× and 1000× alignment markers are formed at the same time.

The gates will not adhere well if there are oxides on the GaAs surface. So, after the PMMA has been patterned, each chip is dipped in a solution of 1:5 30% $NH_4OH:H_2O$ for 5 s to remove these oxides. Removing the oxides is best done immediately before loading in the thermal evaporator so they do not re-form.

The chromium and gold are deposited using a thermal evaporator (Appendix A.6) dedicated[10] for evaporating Cr:Au. The chips are mounted with carbon paint onto a copper stage which is loaded into the evaporator and clamped to an air-cooled platform. A Cr rod (RDM – Item #CRW-2) and one tungsten boat (RDM – Item #S9A-010W) are clamped to the electrical feedthroughs to the evaporator power supply. The tungsten boat is filled with about five 1 mm^3 pieces of Au. After the evaporator chamber has been evacuated to a low vacuum (0.1 mT), the Cr rod is Joule heated briefly to bake out any moisture. The evaporator chamber is evacuated to a medium vacuum (0.5 μT). The stage is covered with an Al-foil shutter, which is opened and closed to allow the desired amount of evaporated metal to coat the chips . The Cr rod and tungsten boat are Joule heated to deposit 50 Å Cr, then 400 Å Au. A crystal monitor is used to measure the thickness of metal deposited. The chips are allowed to cool before being removed from the evaporator.

The lift-off technique is used to remove unwanted metal. The chips are unmounted from the stage and placed in acetone for ~ 1 hour to dissolve the PMMA.

[10] A different stage is used so no Ni, Au, or Ge contaminates the gates and electrically shorts them to the 2DEG.

This lifts off the metal that lay on it, leaving only metal deposited on the GaAs surface. The gates have very fine (dimensions ~ 100 nm) features; so, it is best to avoid use of sonication to aid lift-off. However, if it is necessary, then it is best to minimize the amount of time used. A better remedy is to use a thicker bilayer of PMMA for the next chip. Once lift-off is complete, the chip is blown dry using ultra-high purity nitrogen gas.

Subsection 3.2.6 Ion Milling

Ion milling (Section A.7) is kinematically etching using a directed beam of accelerated argon ions. The ion beam is directed at normal incidence to the sample and has an energy of 500 eV. Shallow (50 nm) etches are used to form regions where the two-dimensional electron gas (2DEG) is permanently depleted. Deep (275 nm) etches are used to expose the AlAs layer, which is etched with hydrofluoric acid to undercut and form free-standing structures. Ion milling has robustly repeatable etch rates and high anisotropy (ratio of vertical to lateral etch distances). These traits allow narrow (~ 100 nm) channels to be defined with ease.

Ion milling etches most materials at approximately the same rate (1 nm/s) because it does not depend on any chemical interactions. The PMMA resist is etched about 1.6 times as quickly as the heterostructure, and it is important the resist is thick enough to survive ion milling. It is best to have resist at least twice as thick as the depth to be etched in the heterostructure. However, if the resist is thicker than 0.3 μm, then the alignment markers are hard to image with the SEM. Due to these limitations, it is

difficult to etch more than 120 nm with good alignment, and deep etches are better accomplished by using a series of shallower etches.[11]

Ion milling for 60 s etches a sufficient depth (~ 50 nm) to deplete the 2DEG. The pattern is defined in a 120 nm thick bilayer of PMMA. The chips are mounted with carbon paint to a stainless steel loading plate. The plate is loaded into the ion miller system (Anand 1995, Spalding 1990) and bolted to a water-cooled target block. The chamber is evacuated to a medium vacuum (1 μT) and then filled with ultra-high purity argon gas to a chamber pressure of 0.2 mT. The Ar atoms are positively ionized by collisions with electrons emitted from a tungsten filament. The argon ions (Ar^+) are accelerated to an energy of 500 eV and directed to the target block.

The PMMA resist is an insulator and can be charged by the Ar^+. If this happens, then the charged PMMA will deflect the Ar^+ beam, reducing the etch rate. To prevent this, a second tungsten filament is used to send electrons to the target with a flux equal to the Ar^+ beam to maintain charge neutrality of the target block.

After etching is complete, the system is left to cool so the hot tungsten filaments do not oxidize from immediate exposure to atmosphere. The loading plate is then detached from the target block, and the chips are removed from the plate. The chip are soaked in acetone for an hour to remove the PMMA resist. An overnight soak is used if all of the PMMA cannot be cleaned off after an hour. If an overnight soak does not suffice, then sonication for brief periods (5 to 10 s) can be used. Using an oxygen reactive ion etch in another method for removing residual PMMA resist.

[11] One trick is to expose the alignment markers by patterning and developing the PMMA above them, and then align to the now more visible alignment markers. The alignment markers will be destroyed by the

Subsection 3.2.7 Oxygen Reactive Ion Etch (descummer)

The oxygen reactive ion etch (Appendix A.8) can clean, or descum, the surface of a chip when soaking in organic solvents fails. It does not etch GaAs, $Al_xGa_{1-x}As$, or metals; however, using it for long periods can oxidize exposed $Al_xGa_{1-x}As$ surfaces. So, it is best to first try cleaning with solvents.

First, the cleaning time (30 to 60 s) and power (70 to 80 W) are set. Then, the chips to be cleaned are placed in the descummer chamber, which is evacuated to a low vacuum (~ 0.2 T). A mass flow controller is opened to fill the chamber with ultra-high purity oxygen gas to a pressure ~ 0.4 to 0.6 T. Once the pressure stabilizes (~ 0.3 to 0.4 T), the gas is ignited into a plasma with pressure ~ 0.5 to 0.6 T. The plasma is automatically quenched once the descummer timer reaches 0, and the chamber is automatically vented. The chips are then removed from the chamber and inspected. If they are not clean, they can be descummed again immediately. Typically 30 to 60 s is sufficient to remove any residual PMMA or surface contaminants, but if the chip is not clean after a cumulative 5 min. of descumming, then the surface contaminants are unlikely to ever be removed.

Subsection 3.2.8 Hydrofluoric Acid Etching

Hydrofluoric acid (Appendix A.9) is used to etch the AlAs sacrificial layer of the heterostructure and create a free-standing structure. Hydrofluoric acid (HF) etching is performed after the AlAs layer has been exposed by ion milling. Hydrofluoric acid etches AlAs up to 10^7 times faster than GaAs (Yablonovitch 1987). So, the GaAs cap

---

etch; so, this should only be employed if the alignment markers are not to be used again.

layers on both sides of the quantum well that contains the two-dimensional electron gas protect it from the HF etch.

The HF concentration (2:15 49% HF:H_2O) used etches AlAs at a rate ~ 200 nm/s, and the etch time is determined by the minimum dimension of the structure to be freed. For example, to free a cantilever 20 μm long and 5 μm wide, the cantilever needs to be left in the HF solution for 15 seconds, which etches 3 μm in from both sides of the cantilever. This totals 6 μm, which spans the width of the cantilever and frees it.

Before etching, all PMMA resist must be cleaned from the surface. Then, the chip to be etched is dipped in solutions of 1:5 NH_4OH: H_2O and 1:5 HCl: H_2O for 10 s each. This removes surface oxides which interfere with the formation of a self-assembled monolayer (SAM) on the chip after HF etching. The SAM passivates the chip and prevents new surface states formed by the HF etch from depleting the 2DEG in the quantum well (Beck 1998b).

After the surface oxides have been removed, the chip is placed on Teflon blocks in a plastic beaker containing 2 ml 49% HF and 15 ml H_2O. After the desired etch time has elapsed, the HF solution is flushed away with 2 liters of distilled water. The SAM is hydrophobic; so, the water is then flushed away with 2 liters of 200 proof ethanol. The chip is then transferred to a plastic beaker containing 15 ml of ~ 5 millimolar solution[12] of $HS(CH_2)_2(CF_2)_{10}CF_3$ in ethanol and left in the $HS(CH_2)_2(CF_2)_{10}CF_3$ solution for at least 48 hrs. to allow the SAM to form.

[12] Grateful thanks are given Joe Tien of the Whitesides group. He provided the most recent sample.

Subsection 3.2.9 Critical Point Drying

The critical point dryer (Appendix A.10) is used to bring a free-standing structure out of a self-assembled monolayer (SAM) solution in ethanol. This is done after hydrofluoric acid etching. The structures cannot be simply blown dry as the surface tension of the liquid underneath the structure will pull it towards the substrate. Once the structure is stuck to the substrate, it cannot be unstuck, and the very structure we wished to free has been destroyed.

The critical point dryer (CPD) exchanges the SAM solution with liquid carbon dioxide (CO_2), which is miscible with ethanol. This is done in a sealed chamber so the temperature and pressure can be controlled. In this way, CO_2 can be taken around its critical point, where its liquid and gaseous phases are indistinguishable. By going around the critical point, CO_2 is taken from its liquid phase to a liquid-gas phase to its gaseous phase without a phase transition. The CO_2 gas can be slowly vented, leaving the structure dry and free-standing.

During the critical point drying process, the chip is kept submerged in ethanol until the ethanol has been exchanged with CO_2. The chip is kept in solution as it is transferred to the CPD chamber, which was partially filled with ethanol beforehand. The chamber is then sealed and cooled to $-10\ ^{\circ}C$. Carbon dioxide gas is introduced into the chamber and condenses when the pressure reaches ~ 400 psi. As the chamber fills with liquid CO_2, the pressure rises to ~ 800 psi. The liquid CO_2 and ethanol are allowed to mix for a few minutes. Then, the chamber is vented until half of the liquid CO_2-ethanol combination has been removed. The chamber is then re-cooled and re-filled with liquid CO_2. This fill-vent process is repeated until all of the ethanol has been purged. At that

point, the chamber is heated to maintain a temperature > 34 °C to bring the CO_2 past its critical point and to prevent the CO_2 from re-condensing. The CO_2 gas is then vented slowly so the CO_2 does not recondense. The chip is removed once the chamber reaches atmospheric pressure.

Subsection 3.2.10 Wirebonding

The wirebonder (Appendix A.11) is used to connect measurement electronics to ohmic contacts and electrostatic gates. The wirebonder bridges the "last millimeter gap" by attaching Au wires to the ohmic contact and gate bonding pads. The wires are ultrasonically soldered to the top Au layer of the ohmic contact and gate bonding pads.

Devices are wirebonded on the sample carriers to be used during measurement. The sample carrier is clamped onto the metal wirebonder stage, which is heated to 80 °C. The user, stage, wirebonder head, and electrical leads on the sample carrier are all electrically connected to earth ground to prevent electrostatic damage to the device.. The wirebonder stage is positioned so the bonding pads of the sample carrier and the device are within the field of motion of the wirebonder head. The head is then brought down to a scanning height a few millimeters above the bonding pads of the sample carrier. After final adjustments to its position, the head is brought down onto the pads. It bonds the Au wire to the pad by pressing on the wire and vibrating side-to-side at a frequency of 2 kHz for a period ~ 1 s. The scan-and-bond procedure is repeated for the device pad, and the wirebonder cuts the wire after this second bond. The bonding process is repeated until all of the pads on the device have been connected to pads on the sample carrier. The sample carrier is then unclamped from the stage, and the electrical leads are disconnected from

earth ground. However, the leads are still connected to each other to prevent voltages from building up.

Section 3.3 Low Temperature Measurements

The "dunker stick" (Berry 1994), the "Shubi Dewar" (Rimberg 1992), and the IR Labs Dewar (Beck 1998b, IRL – Item #HD-3L, Serial #569) were used to perform measurements at low temperatures (T = 4.2 K and 1.7 K). Using the "dunker stick" and "Shubi Dewar" involves immersing the samples in cryogens during measurement. Consequently, these two apparatuses only allows electrical measurements through the wires wirebonded to the device. While quick to use, they are most useful for simple, electrical transport measurements. Samples must be loaded into the IR Labs Dewar, which has a cold plate for cooling devices. There is a larger setup cost, but the samples remain in vacuum. This allows characterization of free-standing cantilevers, which would be destroyed by immersion in cryogens. In addition, there is ample space for external probes such as a piezoelectric bimorph to mechanically excite the device.

Subsection 3.3.1 The "Dunker Stick"

The "dunker stick" is used for electrical transport measurements on devices immersed in liquid ^{4}He. It is a 52" long metal rod with wires running along its length to a chip socket which holds the device to be measured. The "dunker stick" is extremely useful and easy to use for low-temperature measurements. However, the only temperature accessible is T = 4.2 K, and the "Shubi Dewar" and the IR Labs Dewars are

used to access a greater temperature range. This subsection describes the flanges, radiation shielding, and electrical wiring of the "dunker stick".

The "dunker stick" has a Ladish-type flange and a KF40 vacuum flange. The Ladish flange mates the "dunker stick" to the fill port of a liquid He storage Dewar. The Ladish flange lies around a metal sheath, which protects the "dunker stick" wiring from physical damage. The metal sheath is clamped to the "dunker stick" via the KF40 vacuum flange.

The "dunker stick" wiring is enclosed in metal for radiation shielding. There is an outer metal sheath that surrounds the "dunker stick". A thin, hollow brass cylinder is slipped around the sample at the bottom of the "dunker stick" for a second layer of radiation shielding. A series of optically opaque metal baffles and microwave frequency radiation-absorbing foam is used to block radiation from traveling down the length of the "dunker stick".

The wiring consists of three components: the "switcher box" at the top of the dunker stick, the wiring along the length of the "dunker stick", and the chip socket at the bottom of the dunker stick. The "switcher box" mates with the "dunker stick" via a 24-pin Fischer connector and has 24 male, BNC connectors. There is a two-position switch that controls whether the 24 "dunker stick" wires soldered to Fischer connector pins are connected to each other ("GROUND" position) or to the center pins of the BNC connectors ("MEASURE" position). When switching from "GROUND" to "MEASURE", there is a moment when the pins are connected both to each other and to the BNC center pins. This insures that one pin does not develop a voltage relative to another just before they are connected to the device. In addition, there is a three-position

switch for each BNC connector that controls whether the BNC center pin is connected to the shield of the BNC connector ("GROUND" position), floating ("FLOAT" position), or connected to the bus wire ("BUS" position).

Both manganin and copper wires are used in the "dunker stick". Manganin resistive wires are used along most of the length of the "dunker stick" to reduce thermal conduction. They are soldered to the pins of the Fischer connector at the top of the "dunker stick", and run down the length of the "dunker stick" through slots in the optical baffles. At the bottom, each wire is connected to a 1 kΩ resistor, and copper wire is used to connect the other end of the resistor to a pin on a 24-pin chip socket.

The samples are mounted on 5/8 × 5/8 $in.^2$ chip carriers which mate to a chip socket at the bottom of the "dunker stick". The samples are mounted on the chip carrier using GE varnish. A small drop of GE varnish is placed on the chip carrier, and the chip is placed on top of the GE varnish. The end of a wooden applicator stick is used to press the chip onto the carrier. To dry the GE varnish, the chip and carrier are baked in a hot plate oven with hot plate temperature T = 150 °C for an hour.

The procedure for using the "dunker stick" is described below:

1. Remove both sheaths from the "dunker stick" to allow access to the chip socket.
2. Connect the "switcher box" to the "dunker stick" and set the two-position and all the three-position switches to "GROUND". Connect one end of a BNC cable to earth ground through a 10 kΩ resistor. Connect the other end to one of the BNC connectors on the "switcher box".
3. Wearing a grounding strap, push the chip carrier into the chip socket. Hold the chip socket firmly so none of its wires get broken.

4. Slip the brass sheath around the metal prongs holding the chip socket. Then, slide the long, metal sheath up and around the "dunker stick", and clamp the KF40 flanges of the "dunker stick" and sheath together. Slide the Ladish flange around the metal sheath all the way to the bottom of the sheath, *i.e.* the end away from the "switcher box".
5. Disconnect the BNC cable leading to earth ground from the "switcher box".
6. Slowly open the vent valve of the liquid He storage Dewar to release excess pressure.
7. Unclamp the Ladish flange around the fill port of the storage Dewar and remove the Dewar insert.
8. Clamp the Ladish flanges of the "dunker stick" and storage Dewar together.
9. Slowly push the "dunker stick" all the way down into the Dewar. Stop whenever a lot of He gas[13] comes out of the vent valve, and continue once the gas flow abates. Close the vent valve after the "dunker stick" reaches bottom.
10. Connect the measurement electronics to the BNC connectors on the "switcher box", making sure no voltage is being applied to the connectors.
11. For each BNC connector in use, first turn the three-position switches to "FLOAT". Then turn the two-position switch on the "switcher box" to "MEASURE".
12. When done, make sure no voltage is being applied to the "switcher box" BNC connectors, and turn the two-position switch to "GROUND". Then, turn all the three-position switches to the "GROUND" setting.
13. Slowly open the vent valve for the storage Dewar. After all the He gas is vented, unclamp the Ladish flanges and remove the "dunker stick". Re-clamp the Dewar insert to the storage Dewar and close the vent valve.

14. Connect one of the BNC connectors to earth ground as in Step 2 and wait for the "dunker stick" to warm up. Then, wearing a grounding strap, remove the metal sheathes, and extract the chip carrier from the chip socket.

Subsection 3.3.2 The "Shubi Dewar"

The "Shubi Dewar" is a ^{3}He cryostat, but we only describe its use with ^{4}He to attain temperatures as low as T = 1.7 K. Samples are loaded in the "Shubi Dewar" using the "dunker stick" with a different metal sheath that is narrower and has a KF50 vacuum flange instead of a Ladish flange. The narrower metal sheath is used to accommodate the narrower neck of the "Shubi Dewar". The KF50 flange is silver-soldered to the metal sheath to form a vacuum-tight seal. This is required because the lower temperatures are achieved by pumping on the ^{4}He bath.

The procedure for using the "Shubi Dewar" follows below:

1. Load the sample as described for the "dunker stick" and insert the stick into the "Shubi Dewar". Remove the overpressure relief valve and blank off all of the other flanges to the "Shubi Dewar". Insert the fill/flush tube into the fill port, leaving it ~ 1" from the bottom of the Dewar, and use it to fill the "Shubi Dewar" with liquid nitrogen. Wait ~ 1 to 2 hours for the temperature to reach 77 K, monitoring the temperature using two precision resistors[14] inside the "Shubi dewar". Perform any measurements desired at this temperature.
2. Once the temperature reaches T = 77 K, attach a nipple to the open flange, and push the fill/flush tube to the bottom of the Dewar. Then, attach a long piece of latex

[13] From boil-off of the liquid He due to contact with the room temperature "dunker stick".

tubing to the top end of the fill/flush tube and run the tubing to a liquid nitrogen storage Dewar. Introduce He gas into the "Shubi Dewar" through the nipple to pressurize the "Shubi Dewar" to ~ 3 psi. Allow the He gas to flow for ~ 1 min. after there is no more liquid nitrogen coming out of the fill/flush tube before closing the He gas cylinder. Afterwards, remove the fill/flush tube and remove the nipple from the "Shubi Dewar".

3. Turn on the He level meter and fill the "Shubi Dewar" with liquid He. Wait ~ 1/2 hr. for the temperature to reach 4.2 K and then reattach the overpressure relief valve onto the "Shubi Dewar". Perform any measurements desired at this temperature.
4. To attain lower temperatures, pump on the He bath with the Edwards Model 40 mechanical pump. Begin by turning on the pump with the throttle valve between it and the "Shubi Dewar" closed. With the pump on, open the throttle valve slowly enough so the spring-reinforced hose does not become frosted. The temperature can be determined from the He bath pressure, which is measured on two pressure gauges with calibrated temperature markings superimposed. Once the wanted temperature is attained, perform the desired measurements.
5. When done, turn off the mechanical pump and allow the He to boil off. Remove the insert when the Dewar reaches room temperature.

Subsection 3.3.3 IR Labs Dewars

The IR Labs Dewar is used to perform low-temperature characterization of free-stranding cantilevers in a vacuum space. The vacuum space allows room for external

[14] The resistors' values at T = 300 K, 77 K, ad 4.2 K have been previously measured.

probes for a greater variety of measurements. This subsection describes the wiring and cooldown procedure for a Dewar setup for measurements of the resonant frequency of an scanned probe microscopy cantilever fabricated from a GaAs/$Al_xGa_{1-x}As$ heterostructure.

The IR Labs Dewar has a "switcher box" with ten BNC connectors to make electrical contact to the device being measured. The center pins of the connectors are connected to a ten-pin military connector (AEI – Item #PT01A-12-10S) which provides electrical feedthrough to the inside of the Dewar. The Dewar-side pins of the military connector are soldered to miniature coaxial cables to exclude magnetic flux. Five pins are soldered to the center conductors, and five are soldered to the shields. The cables were chosen to be stainless steel for minimal thermal conduction. The other ends of the coaxial cables (center conductor and shields) are soldered to copper wires, which are clamped between two copper blocks bolted to the Dewar cold plate for heat sinking. After passing through the heat-sinking blocks, the wires are soldered to the pins of a ten-pin, male Microtech connector (MCT – Item #GM-10).

A second ten-pin military connector provides electrical contact to the probes. The outside pins of the military connector are soldered to the center pins of ten BNC cables. The shield conductors of the BNC cables are all electrically connected. The inside pins of the military connector are soldered to resistive manganin wires for lower thermal conduction. The manganin wires are wound around and GE varnished to a copper bobbin (LCI – Item #HSB-40), which is bolted to the Dewar cold plate for heat sinking. From the bobbin, the manganin wires are soldered to Microtech connectors, which are connected to another set of Microtech connectors. The pins of the second Microtech connector are soldered to copper wire. The copper wires are wound around and GE

varnished to another heat-sinking bobbin bolted to the Dewar cold plate. The copper wires are then connected to a third and final set of Microtech connectors wired to the probes: a piezoelectric bimorph to mechanically excite the device, a red light-emitting diode (LED) to illuminate the device, a carbon temperature resistor, and a calibrated silicon temperature diode (LCI – Item #DT-470-SD-13-4D).

All of the wiring leads to the sample mount shown Fig. 3.5. The chip is mounted on the Macor block with epoxy. A bimorph underneath the Macor block is used for mechanical excitation. Copper ground planes around the bimorph shield the chip from the electric fields from the bimorph. The sample mount is clamped inside a copper box. This box is bolted to the cold plate of the Dewar and provides additional radiation shielding. The temperature resistor and red LED are GE varnished to the inside of the box. The calibrated silicon diode thermometer is clamped to the outside of the box.

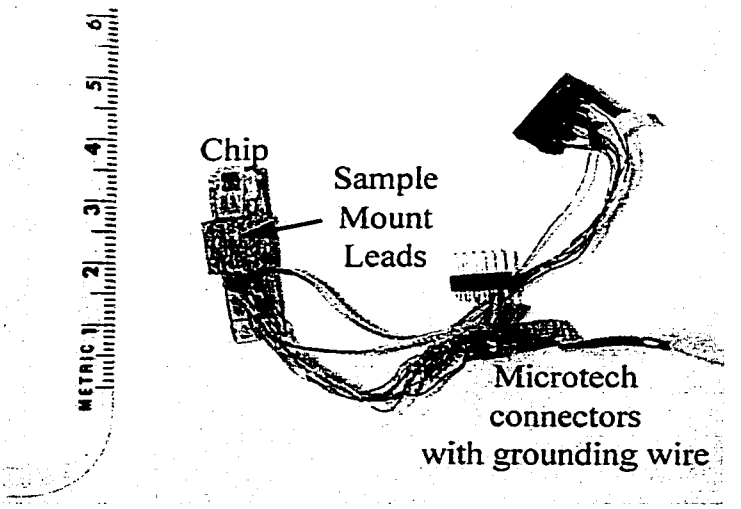

Figure 3.5 Sample mount for the IR Labs Dewar. A chip is mounted and wirebonded to the sample mount leads. The scale is in cm.

The cooldown procedure for the IR labs Dewar is described below:

1. Mount the chip onto the sample mount shown in Fig. 3.5. Plug a ten-pin male Microtech connector with all of the pins soldered together into the female Microtech connector on the sample mount. Use this to electrically connect all of the pins together.
2. Turn the Dewar so the cryogen fill ports point down, and remove the outer cover and nitrogen shield, exposing the cold plate, as seen in Fig. 3.6. In this orientation, the stainless steel coaxial cables leading to the "switcher box" will come in from the right and go towards the center of the cold plate. The probe wires and heat-sinking bobbins are on the left side of the cold plate, and the sample box should sit in the lower right quadrant of the cold plate.
3. Set the two-position switches for both the "switcher box" and the BNC connectors to "GROUND". Connect one of the "switcher box" BNC connectors to a BNC cable connected to earth ground by a 10 kΩ resistor.
4. Attach the Microtech connectors on the sample mount to earth ground, and clamp the sample into the copper box.
5. Turn the copper box on its side and clamp it to the cold plate of the Dewar. Connect the Microtech connectors for the probes.
6. Connect the second set of Microtech connectors on the sample mount to the Microtech connectors inside the Dewar. Then, disconnect the sample mount from earth ground.[15]
7. Screw on the lid of the box, and tape down any loose wires.

[15] Thus, the leads are connected to earth ground at all times – either through the Dewar wiring, or directly through the Microtech connectors.

8. In a star pattern, fasten the screws for the lid for the nitrogen shield, then the screws for the outer can lid.
9. Gently turn the Dewar so the cryogen fill ports are on top, and connect the pressure gauge and military connector for the probes. Then, connect a turbo-mechanical pump to the KF25 flange leading to the chamber. If the turbo-mechanical pump is not available, connect the Edwards Model 5 mechanical vacuum pump.
10. Evacuate the chamber to a pressure of 1 (100) mT with the turbo-mechanical pump (Edwards Model 5 pump).
11. Fill the outer can with liquid nitrogen and wait 10 minutes. In the meantime, the pressure gauge reading should drop to 0.
12. Fill the inner can with liquid nitrogen and wait ~ 1 hour for the temperature to reach 77 K. Use either the carbon resistor resistance (Fig. 3.7) or the silicon diode thermometer to measure the temperature. Perform any measurements desired at this temperature.
13. Attach the fill/flush insert to the inner fill port, and pressurize the inner can with He gas at ~ 3 psi to flush out the liquid nitrogen, similar to the procedure used for the "Shubi Dewar".
14. Fill the inner can with liquid He. The can is full when there is a plume of white smoke that billows out from the inner fill port, not in a cone, but like a fountain.
15. Wait for the temperature to reach T = 4.2 K.
16. Close the valve to the vacuum flange, and turn off and disconnect the pump.
17. Perform any measurements desired at this temperature.

18. To attain lower temperatures, attach the pumping attachment to the inner can fill port, and pump on the He bath with the Edwards Model 5 mechanical pump.
19. Fill the Dewar with cryogens every 12 hours.
20. When done, simply stop adding cryogens and wait for ~ 1 day for the Dewar to warm up. If a faster warm-up is desired, introduce He gas into the vacuum space to a pressure of to ~ 1 T.
21. Once T = 300 K, turn the Dewar upside down, unscrew the lids, and remove the sample mount, with everything electrically connected to earth ground as in Steps 2-6.

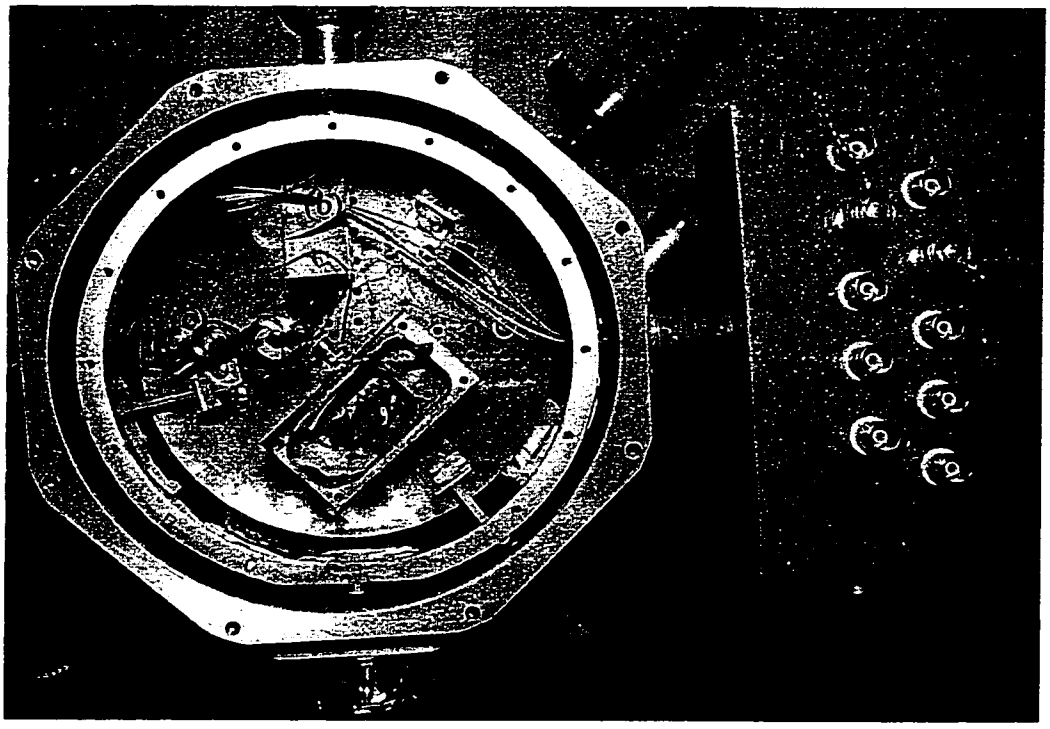

Figure 3.6 Top view of the IR Labs Dewar. (a) "Switcher box" (b) Stainless steel coaxial cables and copper heat-sinking block (c) Probe wires and heat-sinking bobbins (d) Sample box with temperature resistor and LED inside.

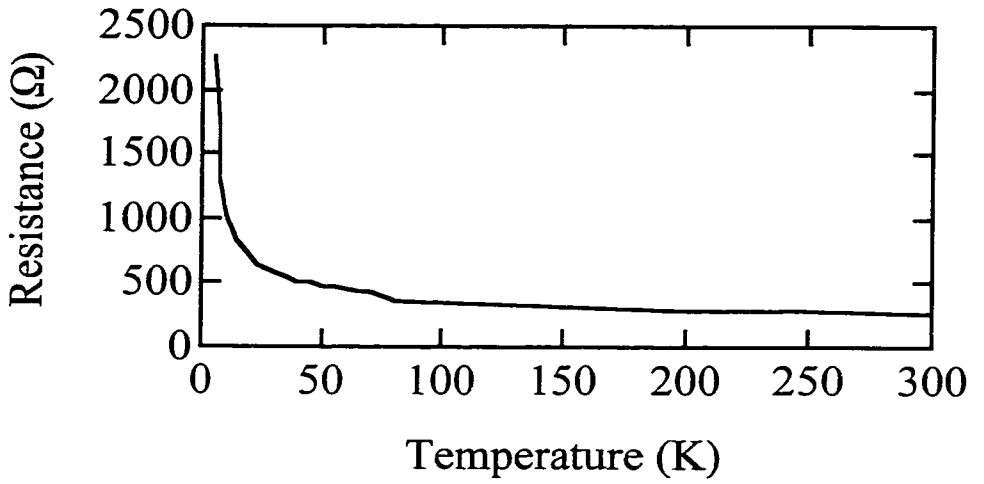

Figure 3.7 Temperature resistor resistance as a function of temperature.

Chapter 4 Charge-Imaging Field- Effect Transistor

In this chapter, we describe the fabrication and characterization of charge-imaging field-effect transistors (FETs). These FETs can be integrated onto a GaAs/AlGaAs scanning probe microscopy (SPM) cantilever (Beck 1998a) to make a movable charge sensor with high spatial resolution. Such a charge sensor is useful for directly imaging the spatial distribution of electrons in small structures.

High spatial resolution ($< 0.1\ \mu m^2$) and excellent charge sensitivity ($\ll 1\ e/Hz^{1/2}$) are obtained by making the FETs with quantum point contact (QPC) geometries. The spatial resolution of the FET was measured at liquid He temperatures using a scanned probe microscope (SPM) with a charged tip (Topinka 2000, 2001a). The charge response of the FET was confined to a disc with full at width half-maximum 340 nm. The charge noise at $T = 4.2$ K has 1/f behavior and reaches values $\ll 1\ e/Hz^{1/2}$ at 30 kHz. In addition, these FETs have low power dissipation ($< 10\ \mu W$), which makes it possible to operate them at He dilution refrigerator temperatures.

This chapter contains eight sections. Section 4.1 describes the heterostructure used, and Section 4.2 outlines the fabrication process. Section 4.3 describes the measurement setups. Sections 4.4 to 4.7 present measurements of the conductance and drain characteristics, the spatial resolution, the charge sensitivity, and the noise spectrum. Section 4.8 summarizes the results.

Section 4.1 GaAs/AlGaAs Heterostructure

The charge-imaging field-effect transistor (FET) was designed for integration onto a free-standing cantilever. The cantilever is defined in a GaAs/AlGaAs heterostructure with an AlAs sacrificial layer. The cantilever is freed by using hydrofluoric acid (HF) to etch the AlAs layer.

Figure 4.1 shows how the heterostructure conduction band edge and composition vary with depth Z below the surface. The heterostructure was grown by molecular beam epitaxy on an undoped GaAs substrate. The heterostructure was designed for constructing free-standing cantilevers with integrated FET sensors. The FETs use a two-dimensional electron gas (2DEG) contained in a quantum well. The quantum well lies 52 nm below the heterostructure surface, and Si δ-doping layers provide carriers for the 2DEG. The quantum well is protected from the hydrofluoric acid etch used to free the cantilever by GaAs cap layers on both sides. The sequence of layers is: 8000 Å of $Al_{0.8}Ga_{0.2}As$ (sacrificial layer for the HF etch), 100 Å of GaAs (cap layer to protect the quantum well), 1510 Å of $Al_{0.3}Ga_{0.7}As$, a Si δ-doping layer (sheet density 1.5×10^{12} cm^{-2}), 220 Å of $Al_{0.3}Ga_{0.7}As$, 200 Å of GaAs (quantum well), 220 Å of $Al_{0.3}Ga_{0.7}As$, a second Si δ-doping layer (sheet density 6×10^{12} cm^{-2}), 250 Å of $Al_{0.3}Ga_{0.7}As$, and 50 Å of GaAs (cap layer to protect the quantum well). This heterostructure is denoted as "Wafer 990924B".[16]

[16] Our collaborators at the University of California, Santa Barbara use the convention "Wafer YYMMDDA" where YY denotes the year, MM the month, DD the day, and A is a letter to order the heterostructures grown that day.

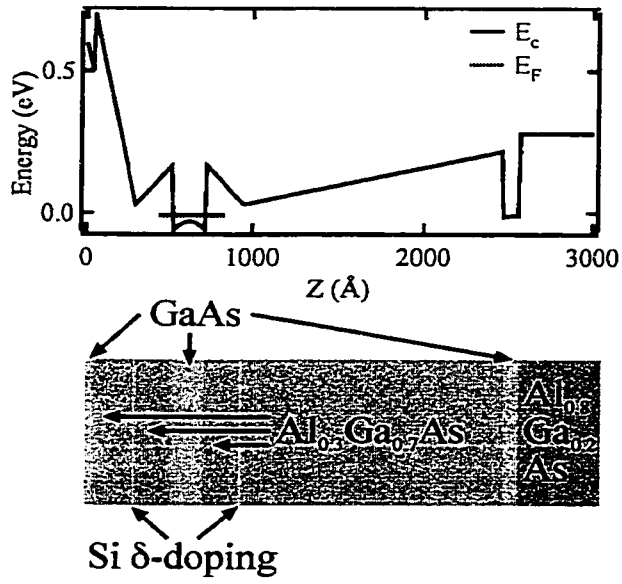

Figure 4.1 Conduction edge and composition of the heterostructure used for the charge-imaging FET. The conduction band edge is plotted as a function of distance Z below the surface, and the dashed line indicates the Fermi level E_F. Both diagrams have been drawn with the same length scale in Z.

The heterostructure contains a two-dimensional electron gas (2DEG) with sheet density $n_s = 8.7 \times 10^{11}$ cm^{-2}. This was determined from the Shubnikhov de Haas oscillation period

$$\Delta_{SdH} = \frac{2e}{hn_s} \tag{4.1}$$

where e is the electron charge, and h is Planck's constant. Shubnikhov de Haas oscillations are oscillations of the longitudinal resistance of a 2DEG as a function of inverse magnetic field. The Shubnikhov de Haas oscillation period $\Delta_{SdH} = 0.055$ T^{-1} was obtained from Fig. 4.2, a plot of the longitudinal resistance of a heterostructure sample as a function of inverse magnetic field at T = 20 mK. The resistance was measured using a PAR 124A lockin amplifier and an Ithaco 1211 pre-amplifier. The measurements were

recorded in the dark at T = 20 mK, and the perpendicular magnetic field was applied using a superconducting solenoid.

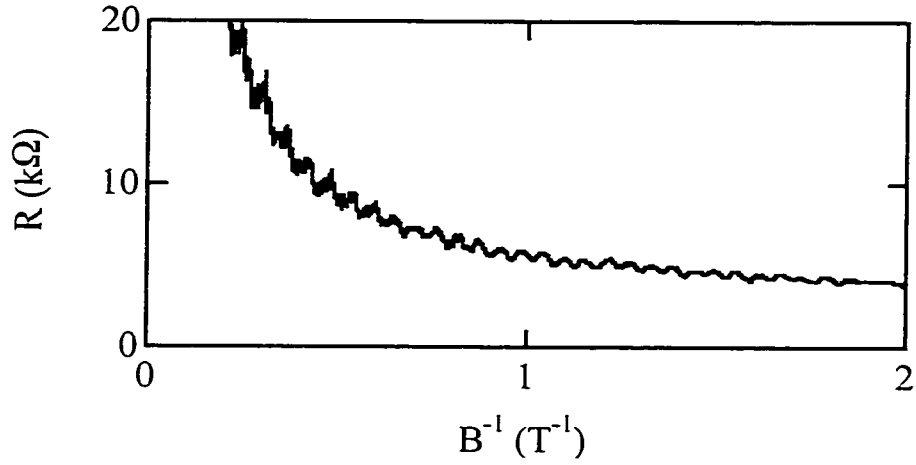

Figure 4.2 Longitudinal resistance R of a sample of the heterostructure denoted "Wafer 990924B" as a function of inverse magnetic field B^{-1} at T = 20 mK. The magnetic field was applied perpendicular to the plane of the sample.

Figure 4.3 is a plot of the conductance of a quantum point contact (QPC) fabricated on the sample as a function of the voltage between the QPC gates and the 2DEG. The conductance plot shows the sheet density $n_s = 1.0 \times 10^{12}$ cm^{-2}, in agreement with the Shubnikhov de Haas oscillation value. The QPC conductance drops sharply when the voltage between the QPC gates and the 2DEG reaches the depletion value

$$V_{depl} = \frac{n_s e d}{\varepsilon} \tag{4.2}$$

where d = 52 nm is the distance between the 2DEG and the gate, and $\varepsilon = 12.54\ \varepsilon_0$ is the dielectric constant of $Al_{0.3}Ga_{0.7}As$ (Blakemore 1987). When the gate voltage $V_g = V_{depl}$, the 2DEG underneath the gates is depleted, and the area under the gates no longer

conducts, causing the sharp conductance drop. From Fig. 4.3, we obtained $V_{depl} = -0.75$ V, which was used to calculate the sheet density n_s.

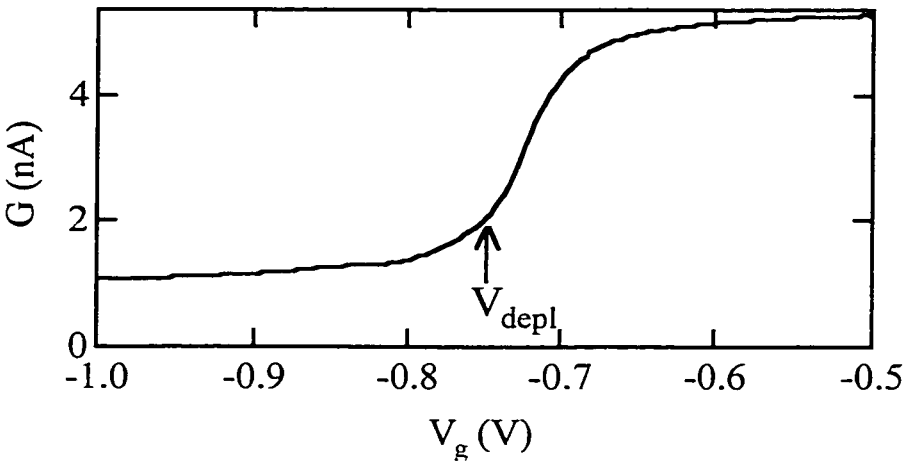

Figure 4.3 Conductance G of a quantum point contact fabricated on a sample of the heterostructure denoted "Wafer 990924B" as a function of gate voltage V_g at T = 20 mK. The arrow indicates the depletion voltage V_{depl}.

Section 4.2 Device Fabrication

Figure 4.4 is a scanning electron microscope (SEM) image of a charge-imaging field-effect transistor (FET) fabricated using the process illustrated in Fig. 4.5. At the top and right of center, the dark gray regions are etch trenches, where the two-dimensional electron gas (2DEG) is permanently destroyed. In the center, the bright feature is the Cr:Au gate, which can electrostatically deplete the 2DEG underneath to form a narrow channel between the gate and the top etch trench. This gives the FET a quantum point contact geometry for high spatial resolution and charge sensitivity.

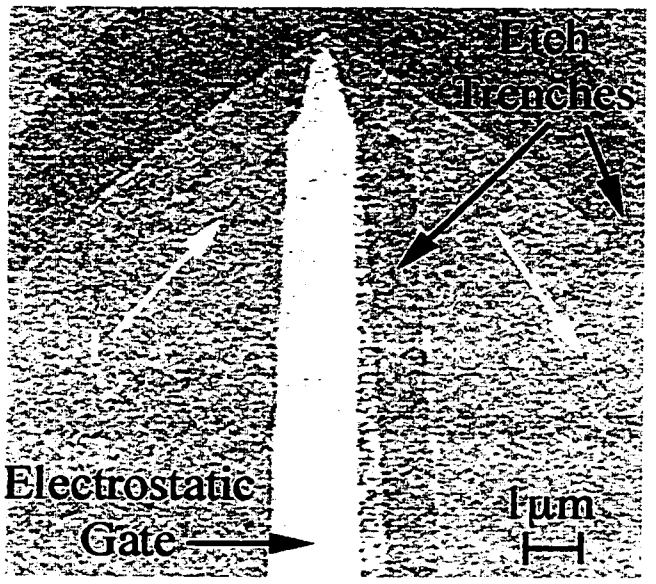

Figure 4.4 Scanning electron microscopy image of the charge-imaging FET. The darker, gray regions are etch trenches, which define a current path indicated by the white arrows. The bright, central feature is the Cr:Au gate, which electrostatically controls the current. Ni:Au:Ge ohmic contacts to the left (drain) and right (source) of the gate have been formed in an area outside the picture.

Figure 4.5 illustrates the series of aligned electron-beam lithography steps (Appendix A) used to fabricate the charge-imaging FET. Figure 4.5(a) shows the first step: forming drain and source ohmic contacts (Appendix A.4) by thermally evaporating Ni, Au, and Ge onto 3×3 mm^2 samples of the heterostructure denoted "Wafer 990924B". A set of large alignment markers was also formed so the features made in subsequent steps were aligned to the ohmic contacts to within 20 μm. Figure 4.5(b) shows the next step, forming electrostatic gates by depositing 5 nm of Cr and 40 nm of Au using thermal evaporation. At the same time, two sets of small alignment markers were formed so subsequent lithography steps could be aligned to the gates to within 100 nm. Figure 4.5(c) shows defining etch trenches by ion milling (Appendix A.7). We directed an argon ion beam with an energy of 500 eV at normal incidence to the sample

for 60 s to etch 50 nm deep trenches. Figure 4.5(d) illustrates depositing 5 nm of Cr and 20 nm of Au by thermal evaporation (Appendix A.6) to from directional markers over a $200 \times 200\ \mu m^2$ area centered around the FET channel. The directional markers were used to position the charge-imaging FET in the scanned probe microscopy system used to measure the FET's spatial resolution and charge sensitivity.

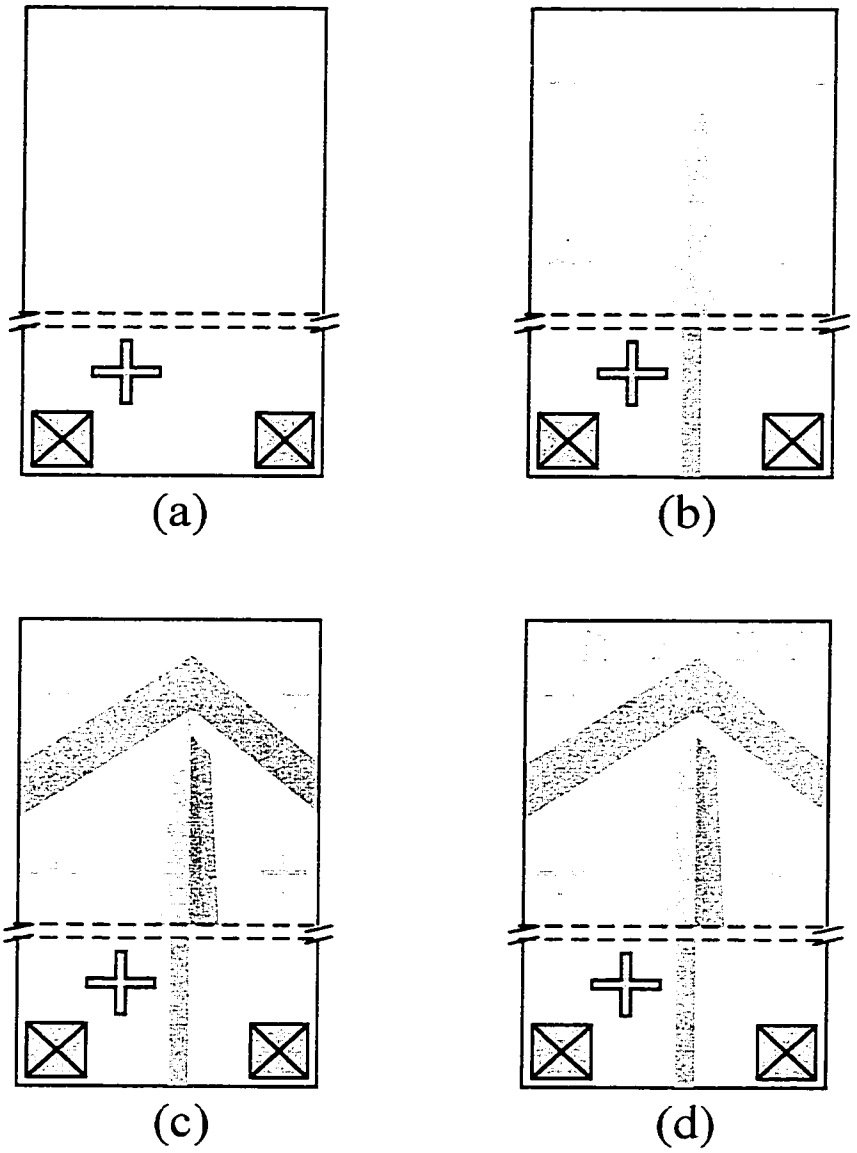

Figure 4.5 Fabrication process for the charge-imaging FET: (a) Ohmic contacts and magnification 20× alignment markers (b) Electrostatic gates and magnification 200× and 1000× alignment markers (c) Etch trenches (d) Directional markers to aid in positioning the SPM tip. The drawing is not to scale.

Section 4.3 Measurement Setups

This section describes how charge-imaging field-effect transistors (FETs) were characterized. Three measurements were performed: conductance and drain characteristics, spatial resolution and charge sensitivity, and noise spectrum.

Subsection 4.3.1 Conductance and Drain Characteristics

Figure 4.6(a) shows the circuit used to measure the channel conductance G of as a function of gate voltage V_g. A PAR 124A lockin Amplifier was used to voltage bias the drain contact of the charge-imaging FET with a 10 μV ac excitation sine wave relative to the source contact. The resulting signal was amplified with an Ithaco 1211 Pre-amplifier, and fed back into the PAR 124A, which amplified the sine wave and integrated it into a dc output signal. The lockin amplifier output was measured using a Fluke 8842A Digital Multi-Meter (DMM). The gate voltage V_g was swept from 0 to –2 V (typical range) using a low-noise voltage source known as the "ramper box" (Katine 1996). The voltage source output was put through a low-pass RC Filter with corner frequency 160 Hz before being applied to the FET gate. The gate voltage was measured with another Fluke DMM. The data from the DMMs were recorded using the "Read N-DMMs" Labview program (Livermore 1998) running on a 7300/200 Power Macintosh computer.

Figure 4.6(b) shows the circuit for measuring the drain characteristics of the charge-imaging FET. All voltages were referenced relative to the FET source ohmic contact. A low-noise voltage source was used to provide a smoothly increasing dc drain-to-source bias voltage. The bias voltage was increased until the current saturated, which typically occurred for $V_{DS} < +1.0$ V. The resulting signal was amplified with an Ithaco

1211 Pre-amplifier. A separate output of the voltage source was put through a low-pass RC Filter with corner frequency 160 Hz before being applied to the FET gate. Both the bias voltage V_{DS} and the signal from the Ithaco Pre-amplifier (I_D) were measured using Fluke 8842A Digital Multimeters (DMMs). The data from the DMMs was recorded using the "Read N-DMMs" Labview program.

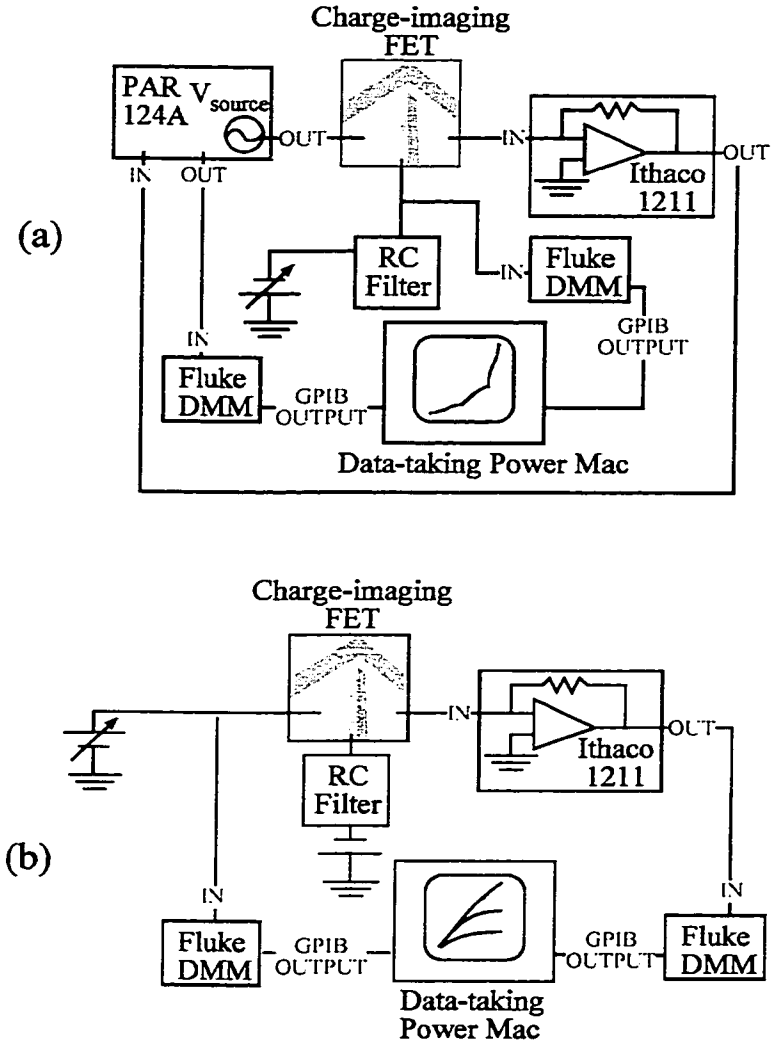

Figure 4.6 Circuits for measuring (a) the conductance (b) the drain characteristics of the charge-imaging FET at T = 4.2 K.

Subsection 4.3.2 Spatial Resolution and Charge Sensitivity

The spatial resolution of the charge-imaging FET was measured using a scanned probe microscope (Eriksson 1997, Topinka 2001b) cooled to liquid He temperatures. The scanned probe microscope (SPM) was both sound and vibration isolated. The SPM has a metal-coated tip which was charged by applying a dc voltage -1.0 V between the tip and the channel. In this way, the tip acts as a charged second gate which capacitively couples to the FET channel, changing the drain current by ΔI_D. The FET was biased in the current-saturation regime and scanned at a constant height 100 nm from the metal-coated tip using a piezoelectric tube. The FET was scanned over a $6.6 \times 6.6\ \mu m^2$ area centered around the FET channel. Measuring the spatially dependent change in drain current ΔI_D yielded the FET's spatial resolution.

Subsection 4.3.3 Noise Spectrum

Figure 4.7(a) shows the circuit used to measure the noise spectrum of the FET when it is voltage-biased. A low noise voltage source was used to provide the drain-to-source bias voltage V_{DS} and the gate-to-source voltage V_{GS}. The values of V_{DS} and V_{GS} were chosen so the FET is in the current saturation regime. The drain current I_D was ac coupled to an Ithaco 1211 Pre-amplifier, which then amplified the remaining signal. The resulting voltage signal was measured using an HP 3561A Spectrum Analyzer. The data from the spectrum analyzer was recorded using the "Measure Noise" Labview VI program (Mar 1994) running on a 7300/200 Power Macintosh computer.

Figure 4.7(b) shows the circuit used to measure noise spectrum of the FET when it is current-biased. The FET was current-biased using a low noise voltage source and a

10 kΩ bias resistor. The drain-to-source voltage was amplified using a PAR 113 Voltage Amplifier, and the amplified signal was measured using an HP 3561A Spectrum Analyzer. The data from the signal analyzer was recorded using a Power Macintosh computer.

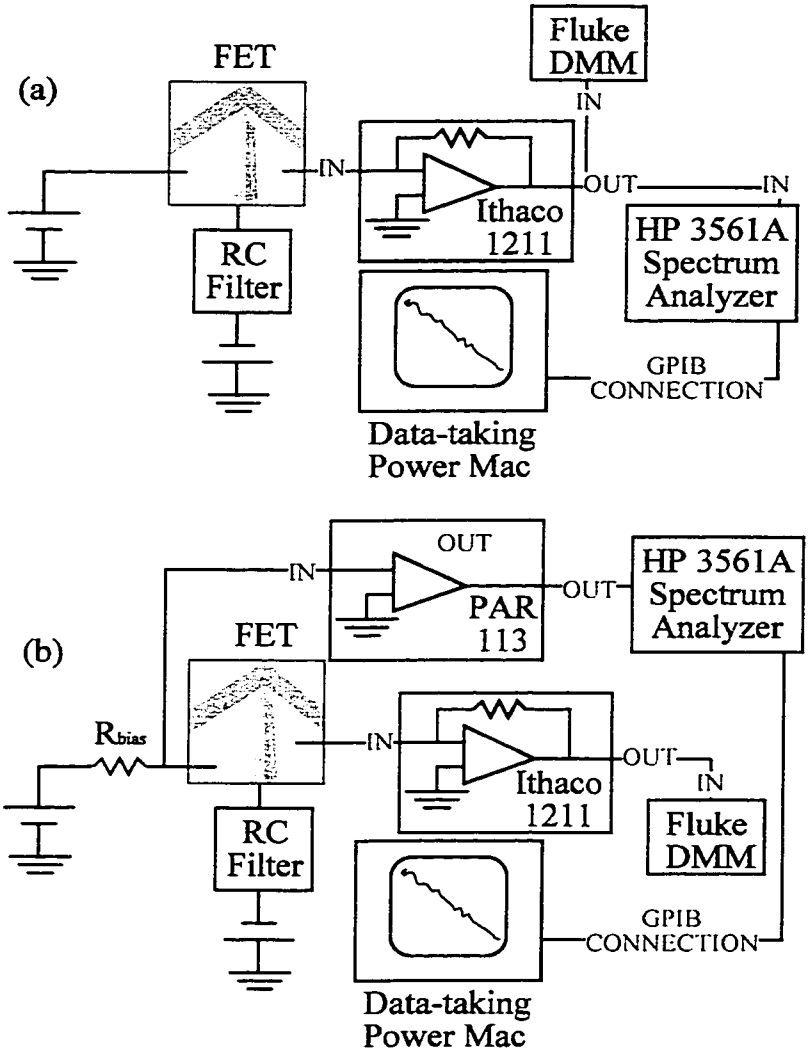

Figure 4.7 Two circuits for measuring the noise spectrum of the charge-imaging FET at T = 4.2 K. The FET is (a) voltage-biased (b) current-biased through its drain contact.

Section 4.4 Conductance and Drain Characteristics

Figure 4.8 plots the charge-imaging FET channel conductance G vs. gate voltage V_g at T = 4.2 K. The conductance G has several steps near the conductance quantum $2e^2/h$, although the conductances are not exactly integer multiples. Thus, the gate, in conjunction with the etch trench, electrostatically defines a quantum point contact (QPC). The QPC is formed when the 2DEG underneath the gate is depleted, for $V_{GS} < -0.8$ V.

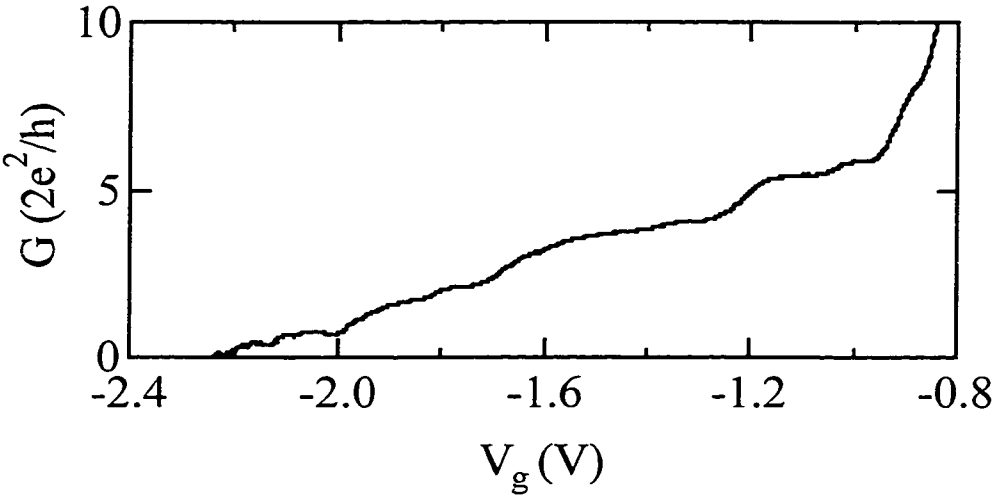

Figure 4.8 Conductance G of the charge-imaging FET as a function of gate voltage V_g at T = 4.2 K. The gate voltage is set relative to the two-dimensional electron gas the FET is formed in.

Figure 4.9 shows the drain characteristics of the charge-imaging FET. The drain current I_D is measured as a function of drain-to-source bias voltages V_{DS} for a series of gate-to-source voltages V_{GS}. The values of V_{DS} shown are sufficient to bring the charge-imaging FET out of the quantum regime, and the drain characteristics are those of a conventional FET – I_D saturates as V_{DS} increases and is controlled by V_{GS}.

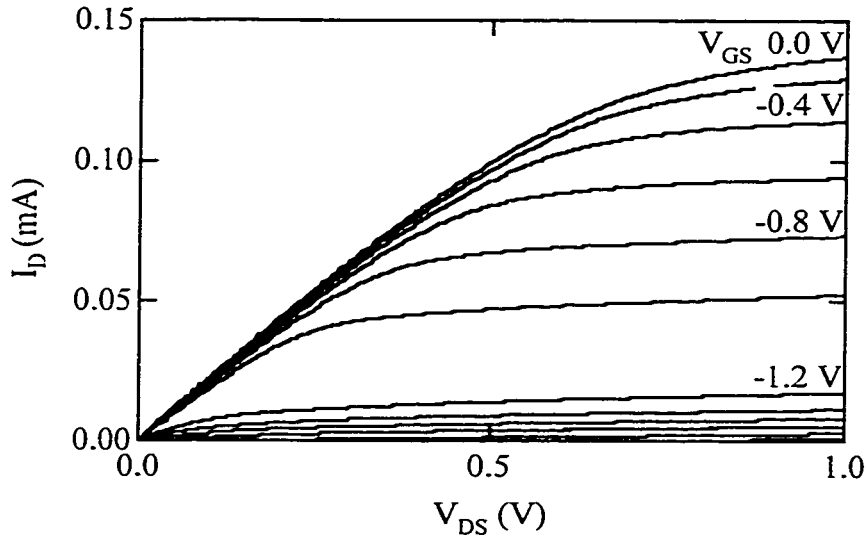

Figure 4.9 Drain characteristics of the charge-imaging FET at T = 4.2 K. The drain current I_D is plotted as a function of the drain-source bias voltage V_{DS} for a series of gate-to-source voltages V_{GS} spaced by –0.2 V. Some curves have been labeled with their V_{GS} value. The drain current I_D saturates smoothly below $V_{DS} = +1.0$ V, a smaller voltage than most commercial FETs.

The drain characteristics determines two characteristic parameters: the transconductance g_m and the small-signal drain-to-source resistance r_{ds}.

$$g_m = \left.\frac{\Delta I_{DS}}{\Delta V_{GS}}\right|_{V_{DS}} \tag{4.3}$$

$$r_{ds} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}} \tag{4.4}$$

The transconductance can be used to estimate the FET's sensitivity to external charges, which will act act as a second FET gate. Thus, the higher the value of the transconductance, the more responsive the FET will be. For the typical operating point $V_{DS} = +1.0$ V and $V_{GS} = -1.0$ V, we find $g_m \approx 20$ μS. The small-signal drain-to-source resistance was found by a linear fit of I_D to V_{DS} for $+0.8 \text{ V} \leq V_{DS} \leq +1.0$ V, using the data from Fig. 4.9. The slope of the fit is the value of r_{ds}, and for a typical operating point of

V_{DS} = +1.0 V, V_{GS} = -1.0 V, r_{ds} ≈ 100 kΩ. The small-signal drain-to-source resistance r_{ds} and the drain lead resistance R_D determine the output impedance $R_{out} = r_{ds} \parallel R_D$ and dimensionless gain $A = g_m R_{out}$. For a typical drain bias resistor of 1MΩ, the output impedance $R_{out} \approx 100$ kΩ and dimensionless gain $A \approx 20$.

Section 4.5 Spatial Resolution

Figures 4.10(a) to (h) show spatial images of the charge-imaging FET's charge sensitivity at T = 4.2 K. The ohmic contact at the left (right) of the image was used as the drain (source) contact, and all voltages are relative to the source contact. The drain-to-source bias voltage was V_{DS} = +1.0 V to put the FET in the current-saturation regime. The white lines in Figs. 4.10(a) to (h) outline the boundaries of the gate and etch trenches, as obtained from a topographic scan of the charge-imaging FET. Comparing Fig. 4.4 and Figs. 4.10(a) to (h), we match the top white line to the upper etch trench, the central angled white line to the gate, and the white line on the right to the side etch trench. In each scan, a gently sloping background signal has been subtracted, and the scale bar represents the percentage change in I_D.

In Figs. 4.10(a) to (c), the FET channel is not defined, and the charge response ΔI_D is distributed over a large area. In Fig. 4.10(a), V_{GS} = 0.0 V, and the charge response is spread over the 900 nm wide conduction channel defined between the etch trenches. In Fig. 4.10(b), V_{GS} = -0.2 V, and ΔI_D is still confined to the area between the etch trenches. In Fig. 4.10(c), V_{GS} = –0.4 V, and the 2DEG underneath the gate is half-depleted. The charge response ΔI_D is now divided between the broad channel between the etch trenches, and the narrower one between the gate and the etch trench.

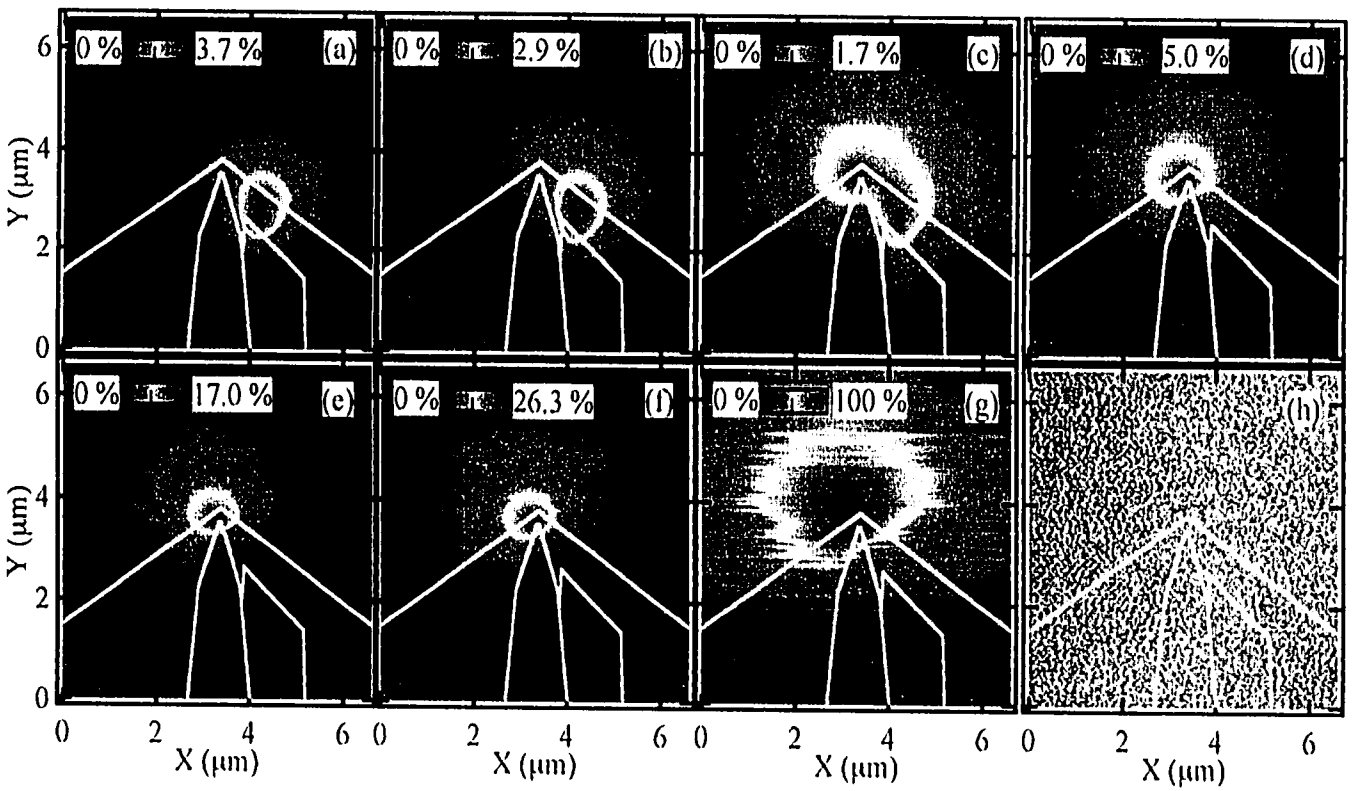

Figure 4.10 Spatial images of charge sensitivity obtained at T = 4.2 K by scanning the FET under a charged metal-coated tip. The ohmic contact to the left (right) of the image is the drain (source) contact. The tip is held at a fixed voltage of -1.0 V, and the FET is voltage-biased with V_{DS} = +1.0 V. A gently sloping background signal has been subtracted from each image, and the scale bar represents the percentage change in the drain current I_D. The half-maximum lies in the center of the bright band. The white lines outline the boundaries of the FET gate and etch trenches, as obtained from a topographic scan: the top white line corresponds to the edge of the etch trench, the central angled white line to the gate, and the white line on the right to the side etch trench. Gate-to-source voltage (a) V_{GS} = 0.0 V (b) V_{GS} = -0.2 V (c) V_{GS} = -0.4 V (d) V_{GS} = -0.6 V (e) V_{GS} = -0.8 V (f) V_{GS} = -1.1 V (g) V_{GS} = -1.7 V (h) V_{GS} = -1.8 V. Absolute change in drain current (a) ΔI_D = 4.0 μA (b) ΔI_D = 2.7 μA (c) ΔI_D = 1.1 μA (d) ΔI_D = 1.5 μA (e) ΔI_D = 2.3 μA (f) ΔI_D = 2.0 μA (g) 5.2 μA (h) N/A.

In Figs. 4.10(d) to (f), the FET channel is defined, and the charge response ΔI_D is maximal between the gate and the etch trench. In Fig. 4.10(d), V_{GS} = -0.6 V, and the two-dimensional electron gas (2DEG) underneath the gate is almost depleted. The maximum of ΔI_D is now in the FET channel. In Fig. 4.10(e), V_{GS} = –0.8 V, which is sufficient to deplete the 2DEG underneath, and the charge response is confined to a small disc between the gate and the etch trench. Also, ΔI_D is a significantly higher percentage of the drain current I_D. In Fig. 4.10(f), V_{GS} = -1.0 V, and the width of the FET channel is electrostatically narrowed by the additional gate voltage. The charge response is confined to a smaller disc and ΔI_D is a higher percentage of I_D.

In Figs. 4.10(g) to (h), there is a loss of spatial resolution as the charge response saturates. In Fig. 4.10(g), V_{GS} = -1.7 V, and the electrical width of the FET channel is almost zero, and there is a large area over which I_D goes to 0. In Fig. 4.10(h), V_{GS} = –1.8 V, and no spatial information can be obtained because the charged tip causes I_D to go to 0 over the entire scan area.

Figs. 4.11(a) to (h) show spatial images of the charge-imaging FET's charge sensitivity with the drain and source contacts reversed from the configuration used in Figs. 4.10(a) to (h). Because of the etch trench on the right of the FET channel, the drain and source contact resistances are unequal. Thus, these images will show any effects of changes in the drain and source resistances. All voltages were still referenced to the source, and the same tip voltage (–1.0 V), tip-to-FET separation (100 nm), and drain-to-source voltage V_{DS} (+1.0 V) were used.

In Figs. 4.11(a) to (c), the FET channel is not formed, and the charge response is divided between the FET channel and the channel between the two etch trenches. In

Fig. 4.11(a), $V_{GS} = 0.0$ V, and the charge response is spread out over the broad channel between the etch trenches. In Fig. 4.11(b), $V_{GS} = -0.2$ V, and the channel is starting to form. The response is divided between the channel between the etch trenches and the channel between the gate and the etch trenches. In Fig. 4.11(c), the charge response ΔI_D is roughly centered in the FET channel, but it spans an region much larger than the channel area.

In Figs. 4.11(d) to (f), the FET channel is formed, and the size of the charge response area decreases as the channel width is narrowed. In Fig. 4.11(d), $V_{GS} = -0.6$ V, and the charge response is centered in the FET channel, and becoming circular. In Fig. 4.11(e), $V_{GS} = -0.8$ V, and the two-dimensional electron gas underneath the gate is depleted. The charge response is now confined to a disc centered between the gate and the etch trench, just as in Fig. 4.10(e). In Fig. 4.11(f), $V_{GS} = -1.1$ V, and the size of the disc has decreased.

In Figs. 4.11(g) to (h), the FET channel is pinched off, again leading to a loss of spatial resolution. In Fig. 4.11(g), $V_{GS} = -1.7$ V, and there are sizeable areas where I_D goes to 0. In Figs. 4.11(h), $V_{GS} = -1.8$ V, and the drain current is zero over almost the entire image area.

Changes in the drain and source resistances have little effect on the charge-imaging FET's performance. The spatial resolution and charge sensitivity are determined by the channel width and the operating point set by the values of V_{GS} and V_{DS}.

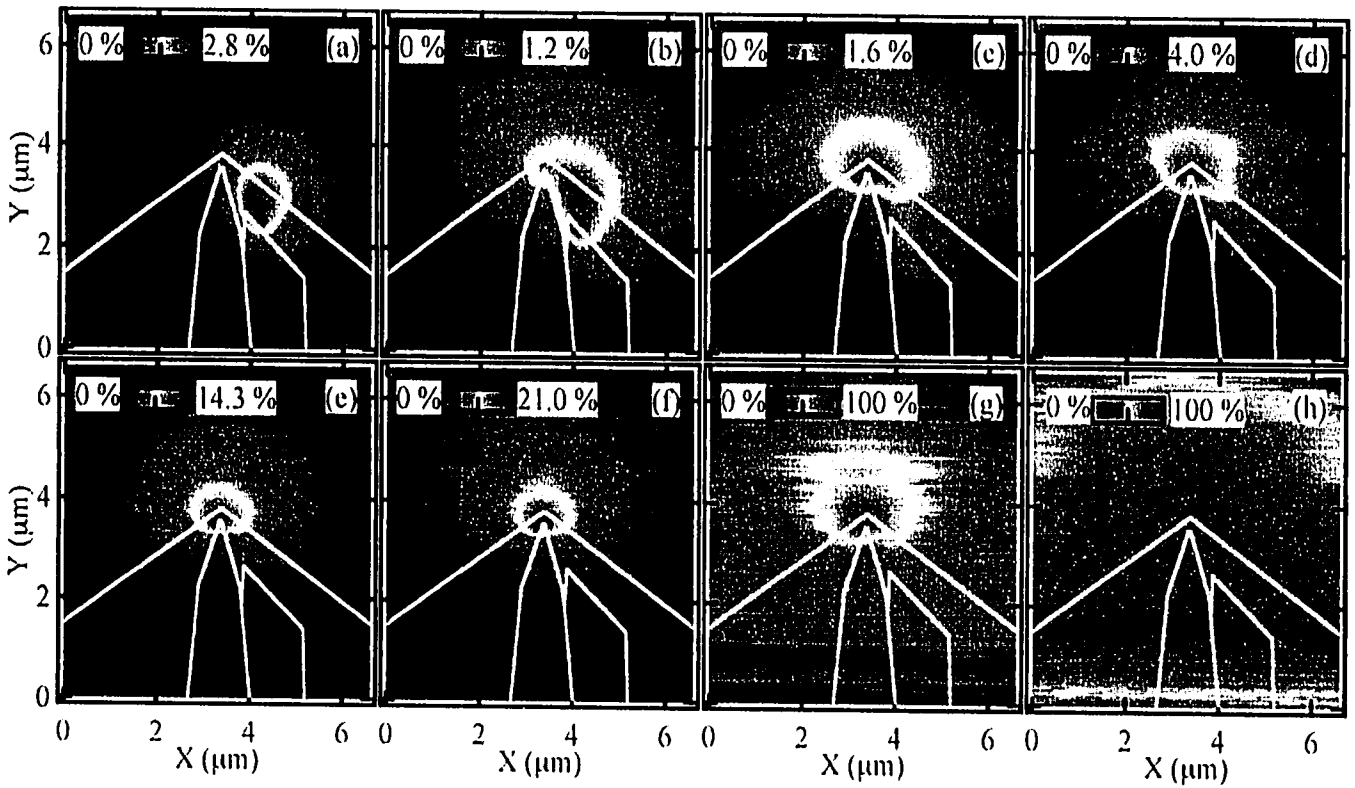

Figure 4.11 Spatial images of charge sensitivity obtained at T = 4.2 K by scanning the FET under a charged metal-coated tip. The ohmic contact to the right (left) of the image is the drain (source) contact. The tip is held at a fixed voltage of -1.0 V, and the FET is voltage-biased with V_{DS} = +1.0 V. A gently sloping background signal has been subtracted from each image, and the scale bar represents the percentage change in the drain current I_D. The half-maximum lies in the center of the bright band. The white lines outline the boundaries of the FET gate and etch trenches, as obtained from a topographic scan: the top white line corresponds to the edge of the etch trench, the central angled white line to the gate, and the white line on the right to the side etch trench. Gate-to-source voltage (a) V_{GS} = 0.0 V (b) V_{GS} = -0.2 V (c) V_{GS} = -0.4 V (d) V_{GS} = -0.6 V (e) V_{GS} = -0.8 V (f) V_{GS} = -1.1 V (g) V_{GS} = -1.7 V (h) V_{GS} = -1.8 V. Absolute change in drain current (a) ΔI_D = 3.5 μA (b) ΔI_D = 1.4 μA (c) ΔI_D = 1.2 μA (d) ΔI_D = 1.3 μA (e) ΔI_D = 2.2 μA (f) ΔI_D = 2.0 μA (g) ΔI_D = 1.1 μA (h) ΔI_D = 1.3 μA.

To determine the spatial resolution of the FET, we use the full width at half-maximum (FWHM) of the sensitive regions in Figs. 4.10(a) to (h). Previous work (Eriksson 1996) has shown the charged tip induces a Lorentzian-shaped change in 2DEG sheet density beneath the tip with FWHM equal to twice the spacing between the tip and the 2DEG. This spacing was 150 nm for the Figs. 4.10(a) to (h); so, to obtain the spatial resolution Δr of the FET alone, a Lorentzian of FWHM 300 nm was deconvolved from Figs. 4.10(a) to (h). For Fig. 4.10(a), we obtain Δr = 850 nm, comparable to the lithographic distance 900 nm between the two etch trenches, as measured from Fig. 4.4. For Figs. 4.10(e) to (f), we obtain Δr = 340 nm, comparable to the lithographic distance 250 nm between the gate and the etch trench, as measured from Fig. 4.4. Thus, the spatial resolution of the charge-imaging FET is determined by its channel width.

Section 4.6 Charge Sensitivity

Three different estimates show the scanned probe microscope tip induced a charge ≈ 60 electrons in the FET channel. A rough estimate is from modeling the tip and FET channel as two metal spheres. The capacitance C_{12} between two spheres separated by vacuum is (Corson 1970)

$$C_{12} = 4\pi\varepsilon_0 \frac{r_1 r_2}{D}(1-\alpha^2)\sum_{n=0}^{\infty}\frac{\alpha^n}{1-\alpha^{2(n+1)}}, \alpha = \frac{\beta-\sqrt{\beta^2-4}}{2}, \beta = \frac{D^2-r_1^2-r_2^2}{r_1 r_2} \qquad (4.5)$$

where D = 150 nm is the distance between the spheres, and r_1 = 125 nm and r_2 = 125 nm are the radii of the two spheres. If a dielectric layer of thickness d is placed between the two spheres, Eq. 4.4 must be multiplied by the pre-factor

$$\frac{(D-r_1-r_2)\varepsilon}{(D-r_1-r_2-d)\varepsilon+d\varepsilon_0} \tag{4.6}$$

to give the capacitance C_{12} between the two spheres. The FET channel depth d = 52 nm, and the dielectric constant of $Al_{0.3}G_{0.7}As$ is $\varepsilon = 12.54\ \varepsilon_0$ (Blakemore 1987). Equations 4.4 and 4.5 yield a tip-to-channel capacitance C_{12} = 10 aF, which means charging the tip to –1.0 V induces 60 electrons in FET channel.

Describing the FET channel as part of a two-dimensional electron gas (2DEG) with finite electron density shows the tip induced 50 electrons in the FET channel. Previous calculations for the change in the local 2DEG sheet density n_s results in the following expression for the tip-channel capacitance C_{tC} (Eriksson 1996)

$$C_{tC} = \int_0^{2\pi} \frac{n_s}{V_{depl}} \left(\int_0^{r_2} \frac{\rho}{1+(\rho/D)^2} d\rho \right) d\theta \tag{4.7}$$

when the tip lies on the heterostructure surface. The integral is over the area of the FET channel (r_2 = 125 nm), V_{depl} = -0.8 V is the voltage at which the gate depletes the 2DEG underneath, $n_s = 9 \times 10^{11}$ cm^{-2}, and D = 150 nm is the distance between the tip and the channel. The tip was at a height 100 nm above the FET, and to account for the separation, Eq. 4.6 must be multiplied by:

$$\frac{D\varepsilon}{(D-d)\varepsilon+d\varepsilon_0} \tag{4.8}$$

where d = 52 nm is the depth of the FET channel, and $\varepsilon = 12.54\ \varepsilon_0$ is the dielectric constant of $Al_{0.3}G_{0.7}As$ (Blakemore 1987). Equations 4.7 and 4.8 yield a tip-to-channel

capacitance $C_{tC} = 8$ aF. For the tip voltage used, this corresponds to 50 electrons induced in the channel.

Finally, a numerical Poisson simulation (LeRoy 2001, Topinka 2000b) showed the tip induced a charge of 55 electrons in the FET channel. The simulation spanned a 1 μm^3 volume centered in the FET channel. The charged tip was described as a metal cone of angle 30° terminating in a sphere of radius 50 nm. The FET channel was described as a metal disc of radius 250 nm (channel width) and height 20 nm (2DEG thickness). The dielectric constant was $\varepsilon = 12.54\ \varepsilon_0$. The simulation calculated to a tip-channel capacitance $C_{tC} = 9$ aF, which means the a tip voltage of -1.0 V induced 55 electrons in the channel.

Three independent methods arrive at the value of 60 electrons for the charge induced in the channel. The charge response ΔI_D reached values equal to I_D. Therefore, an induced charge of 1 electron should correspond to $\Delta I_D \approx 2$ %.

Section 4.7 Noise Spectrum

Figure 4.12 plots the spectrum of current noise for the charge-imaging FET at $T = 4.2$ K. The spectrum shows 1/f behavior[17] and reaches a noise level ~ 50 pA/Hz$^{1/2}$ at 30 kHz. The FET was voltage biased with drain-to-source voltage $V_{DS} = +1.0$ V. The gate-to-source voltage was held at $V_{GS} = -1.1$ V. A separate measurement with the FET current biased yielded a noise spectrum that matched Fig. 4.12 extremely well.

[17] The power of the fall-off is 1.3, and these deviations may be due to the short channel length (Uren 1985) and switching noise (Burgess 1965, Savelli 1983).

The equivalent charge noise level is $q_n = 1.5 \times 10^{-3}$ e/Hz$^{1/2}$ at 30 kHz. The charge noise q_n can be expressed in terms of the capacitance between the gate and the channel C_{gc} and the transconductance g_m.

$$q_n = \frac{I_n C_{gc}}{g_m} \tag{4.10}$$

The capacitance C_{gc} is difficult to calculate, but modeling the channel as a sphere with radius of 340 nm (FWHM of the charge response) gives $C_{gc} \sim 500$ aF. The transconductance was previously measured to be $g_m = 20$ μS.

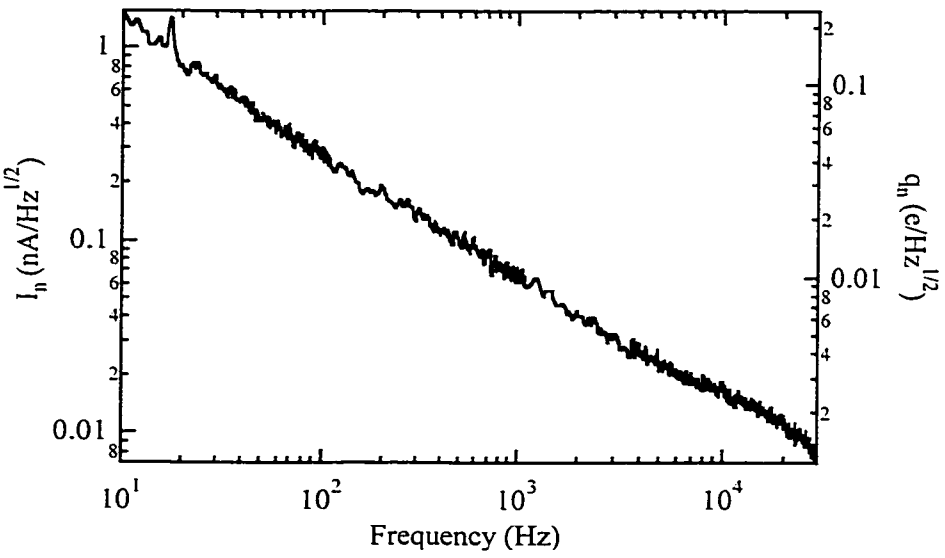

Figure 4.12 Noise spectrum for the charge-imaging FET. The drain-to-source bias voltage was $V_{DS} = +1.0$ V, and the gate-to-source voltage was $V_{GS} = -1.1$ V.

Section 4.8 Summary

In conclusion, we have fabricated a charge-imaging FET with high spatial resolution and excellent charge sensitivity. These FETs can be integrated onto a GaAs/AlGaAs scanning probe microscopy cantilever to make a movable charge sensor. The FET was fabricated using aligned electron-beam lithography steps, and has a quantum point contact geometry. Traces of the channel conductance as a function of gate voltage show steps nears multiples of the conductance quantum ($2e^2/h$) as the channel width is increased. The measured drain characteristics are similar to those of a conventional FET - the drain current I_D saturates smoothly with increased V_{DS} and is controlled by the gate-to-source voltage V_{GS}. The FET's charge response is confined to a disc with full width half maximum comparable to its channel width. The FET charge noise spectrum reaches values « 1 $e/Hz^{1/2}$ at 30 kHz. These FETs offer several advantages for charge-imaging: small channel area (< 0.1 μm^2) for high spatial resolution, excellent charge sensitivity (« $1e/Hz^{1/2}$), and low power dissipation (< 10 μW) for operation at He dilution refrigerator temperatures.

Chapter 5 Scanned Probe Microscopy Cantilevers for Simultaneous Charge-Imaging and Strain-Sensing

This chapter describes the fabrication and measurements of scanned probe microscopy cantilevers designed for simultaneous charge-imaging and strain-sensing. These cantilevers are designed for imaging the spatial distribution of electric charge of a sample and simultaneously mapping the topography in which the charge lies.

Charge-imaging and strain-sensing can be accomplished with field-effect transistors (FETs) integrated onto the cantilever. The strain-sensing FET make the cantilever a topography-imager, and we have fabricated strain-sensing FETs with a vertical deflection noise of 0.5 nm/$Hz^{1/2}$ at 10 kHz. The strain-sensing FET lies at the base of the cantilever, where deflections to the cantilever cause the maximum strain. The charge-imaging FET channel lies at the tip of the cantilever to be sensitive to charges near the cantilever tip.

The chapter is divided into five sections. Section 5.1 discusses the heterostructure material the cantilevers were fabricated from and the process for making the cantilevers. Section 5.2 presents different cantilevers designed for simultaneous charge-imaging and strain-sensing using integrated FETs. Section 5.3 describes the measurement setups. Section 5.4 presents measurements of the drain characteristics, noise spectrum, and response to mechanical excitations of the strain-sensing FET. Section 5.5 summarizes the experimental results.

Section 5.1 Heterostructure Material and Fabrication

The GaAs/AlGaAs heterostructures were designed for the fabrication of free-standing cantilevers with integrated field-effect transistors (FETs) (Beck 1996, 1998). A free-standing cantilever with an integrated strain-sensing FET is shown in Fig. 5.1, which also shows the heterostructure layers near the surface.

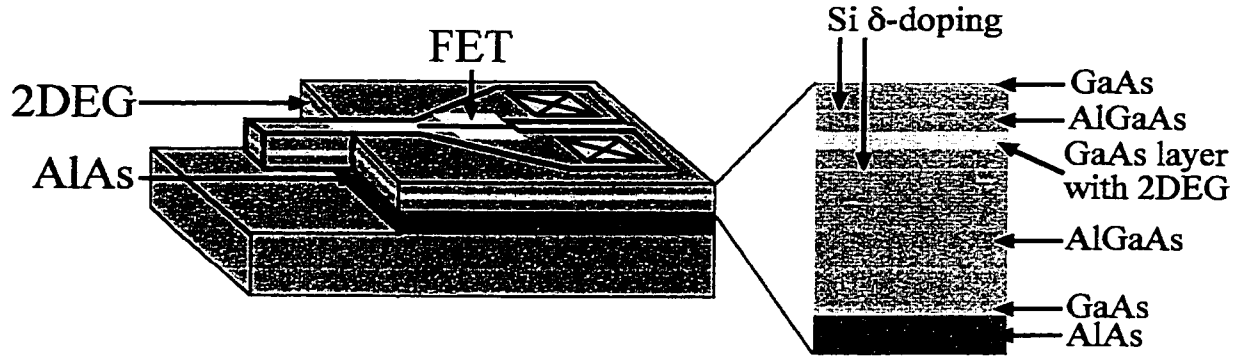

Figure 5.1 Free-standing cantilever with integrated strain-sensing FET and the layers of the heterostructure the cantilever is fabricated in.

Two key features of the heterostructure are the AlAs sacrificial layer and the quantum well which contains a two-dimensional electron gas (2DEG). The AlAs layer is etched with hydrofluoric acid (HF) to free a cantilever defined in the heterostructure. The quantum well confines the 2DEG at the significant voltages (~ 1 V) used to bias the FET (Mar 1994), and is protected from the HF etch by GaAs cap layers on both sides of the quantum well. Two heterostructures were used to fabricate cantilevers with integrated FETs, and the sequence of layers going down from the top surface is outlined in Table 5.1. The heterostructures are denoted as "Wafer 960220C" and "Wafer 990924B" and contain 2DEGs with sheet densities of 1×10^{12} cm^{-2} and 9×10^{11} cm^{-2}, respectively,

as measured from the conductance of quantum point contacts fabricated on samples of the heterostructures.

Wafer 960220C	Wafer 990924B	Purpose
50 Å GaAs	50 Å GaAs	Cap Layer
250 Å $Al_{0.2}Ga_{0.8}As$	250 Å $Al_{0.3}Ga_{0.7}As$	
8×10^{-12} cm^{-2} Si	6×10^{-12} cm^{-2} Si	δ-doping
220 Å $Al_{0.2}Ga_{0.8}As$	220 Å $Al_{0.3}Ga_{0.7}As$	
200 Å GaAs	200 Å GaAs	Quantum Well
220 Å $Al_{0.2}Ga_{0.8}As$	220 Å $Al_{0.3}Ga_{0.7}As$	
2×10^{-12} cm^{-2} Si	1.5×10^{-12} cm^{-2} Si	δ-doping
1510 Å $Al_{0.2}Ga_{0.8}As$	1510 Å $Al_{0.3}Ga_{0.7}As$	
100 Å GaAs	100 Å GaAs	Cap Layer
3000 Å AlAs	8000 Å $Al_{0.8}Ga_{0.2}As$	Sacrificial Layer for Etch
GaAs	GaAs	Substrate

Table 5.1 Sequence of layers for heterostructures used for the construction of free-standing cantilevers with integrated field-effect transistors.

The charge-imaging and strain-sensing cantilevers were fabricated in a series of aligned, electron-beam lithography (Appendix A.3) steps, as illustrated in Figs. 5.2 and 5.3. Figure 5.2 illustrates the fabrication process for cantilevers fabricated from the heterostructure denoted "Wafer 960220C", and for simplicity, only the strain-sensing FET is shown. The fabrication process began (Fig. 5.2 (a)) with forming alignment markers for use at magnification 20×, 200×, and 1000× to allow subsequent steps to be aligned to each other to within 100 nm. The alignment markers were patterned as crosses and formed by thermally depositing 5 nm of Cr and 40 nm of Au (Appendix A.6). Figure 5.2(b) shows the next step, forming drain and source ohmic contacts by thermally evaporating Ni. Au, and Ge (Appendix A.4) and annealing (Appendix A.5) the deposited metal. Figure 5.2(c) shows by ion milling (Appendix A.7)

to define separate conduction paths for the FETs and the outline of the cantilever. Ion milling is a dry etch process that uses a beam of argon ions directed at normal incidence to the sample. We directed an ion beam with an energy of 500 eV towards the sample for 85 s to create 75 nm deep etch trenches. Figure 5.2(d) show thermally depositing (Appendix A.6) 20 nm of Cr and 100 nm of Au to form electrostatic gates. The cantilever and FETs are now defined, and the next stage is to free the cantilever by etching the AlAs layer underneath. The AlAs layer must first be exposed by ion milling (Appendix A.7) for 260 s to etch a depth of 255 nm, as shown in Fig. 5.2(e). The sample was placed in 3:15 49% HF:H_20 for 30 s to etch the AlAs layer and undercut the cantilever, as shown in Fig. 5.2(f). The sample was then submerged in a 5 millimolar solution of $HS(CH_2)_2(CF_2)_{10}CF_3$ in ethanol for 48 hrs. to form a self-assembled monolayer. The $HS(CH_2)_2(CF_2)_{10}CF_3$ monolayer passivates the exposed AlAs and satisfies the additional surface states created by undercutting the cantilever. The free-standing cantilever was brought out of solution by critical point drying (Appendix A.10).

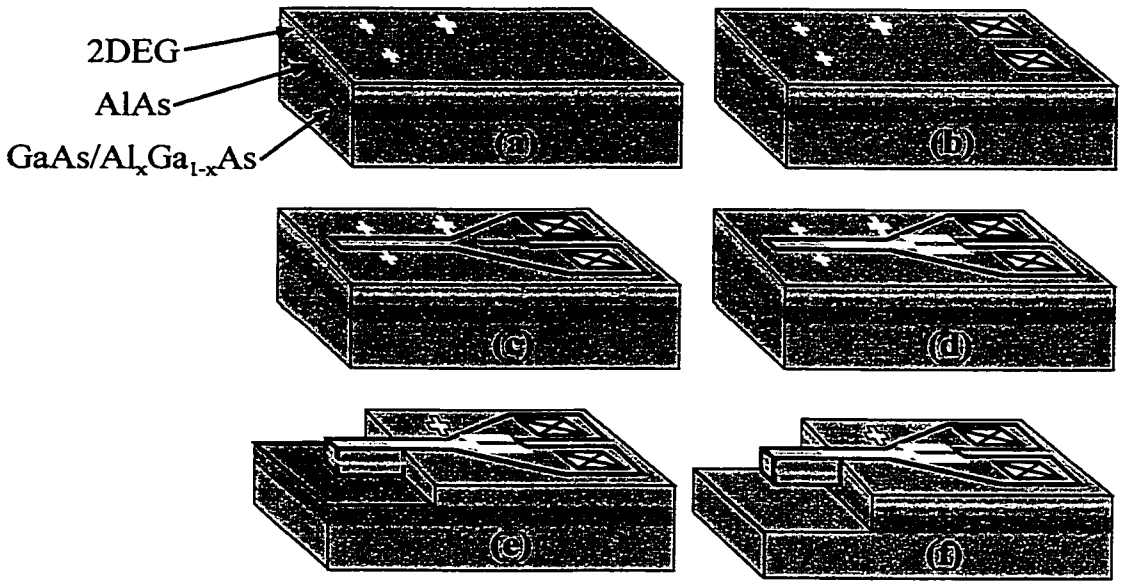

Figure 5.2 Fabrication process for cantilevers made from the heterostructure denoted Wafer 960220C. (a) Magnification 20×, 200×, and 1000× alignment markers. (b) Ohmic contacts. (c) Etch trenches to define FET channel. (d) Electrostatic gates. (e) Etching to defining the cantilever and exposing the AlAs layer. (f) Freeing the cantilever with a hydrofluoric acid etch.

The fabrication process illustrated in Fig. 5.2 proved to be somewhat cumbersome, and the yield was somewhat low (~ 10%). There were difficulties in aligning the gates and removing the PMMA resist before etching with hydrofluoric acid. The gates pass over the etch trenches; so, thicker layers of metal had to be deposited. As a result, the gates needed to be patterned in a thicker layer of PMMA, making it difficult to image the alignment markers during lithography. Second, ion milling for a long time (260 s to expose the AlAs layer) cross-links the PMMA, which then becomes difficult to remove. The residual PMMA created difficulties in wirebonding (Appendix A.11) leads to the cantilevers.

To simplify the fabrication process and improve the yield (~ 40 %) of the charge-imaging and strain-sensing cantilevers, the fabrication steps were changed to the process illustrated in Fig. 5.3. First, the design was altered so the gates no longer pass over the etch trenches. This not only improved alignment by allowing use of a thinner PMMA resist, but also assured continuity of the gates. Second, the ion the deep etch step to expose the AlAs layer was split into two, shallower etches. Shortening the ion milling time prevents the PMMA from being cross-linked, and greatly simplified removing the PMMA in preparation for etching with hydrofluoric acid.

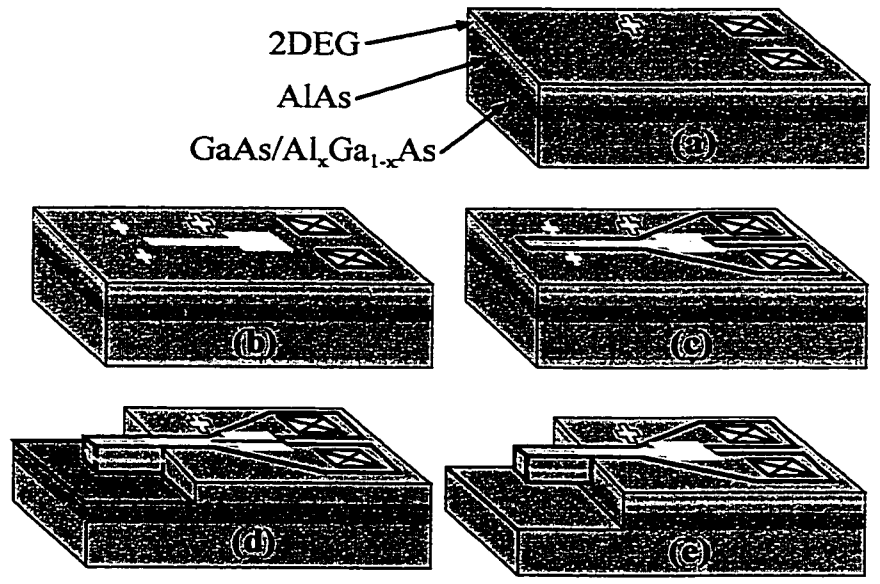

Figure 5.3 Fabrication process for cantilevers made from the heterostructure denoted Wafer 990924B. (a) Ohmic contacts and magnification 20× alignment markers. (b) Electrostatic gates and magnification 200× and 1000× alignment markers. (c) Etching to define the FET channel. (d) Etching to define the cantilever and expose the AlAs layer. (e) Freeing the cantilever by etching the AlAs layer with hydrofluoric acid.

The fabrication process illustrated in Fig. 5.3 was used for fabricating cantilevers from the heterostructure denoted "Wafer 990924B". Figure 5.3(a) illustrates the formation of the drain and source ohmic contacts and the magnification 20× alignment markers. The contacts and markers were patterned in a trilayer of PMMA, and Ni, Au, and Ge were thermally deposited (Appendix A.4) and annealed (Appendix A.5). The markers allow subsequent steps to be aligned to the ohmic contacts to within 20 μm. Figure 5.3(b) shows the next step, thermally depositing 5 nm of Cr and 40 nm of Au (Appendix A.6) to form the electrostatic gates and the magnification 200×, 1000× alignment markers. The markers allow subsequent steps to be aligned to the gates to within 100 nm. Next, etch trenches to define the conduction channel for the FET and the outline of the cantilever are formed by ion milling (Appendix A.7), as illustrated in Fig. 5.3(c). We directed an argon ion beam with an energy of 500 eV for 70 s to form 60 nm deep etch trenches. To expose the AlAs layer, ion milling for 120 s is repeated twice. Each time, 100 nm is etched, and combined with the previous etch (Fig. 5.3(c)), a total depth of 260 nm is etched, sufficient to expose the AlAs layer, as shown in Fig. 5.3(d). The sample was placed in 2:15 49% HF:H_20 for 45 s to etch the AlAs layer and undercut the cantilever, as shown in Fig. 5.3(e). The sample was then submerged in a 5 millimolar solution of $HS(CH_2)_2(CF_2)_{10}CF_3$ in ethanol for 48 hrs. to form a self-assembled monolayer. The $HS(CH_2)_2(CF_2)_{10}CF_3$ monolayer passivates the exposed AlAs and satisfies the additional surface states created by undercutting the cantilever. The free-standing cantilever was brought out of solution by critical point drying (Appendix A.10).

Section 5.2 Fabricated Cantilevers

Figure 5.4(a) is a scanning electron microscope (SEM) image of a free-standing cantilever with integrated charge-imaging and strain-sensing FETs. The bright, angled line around the edge of the cantilever is the gate for a charge-imaging FET, and the bright rectangle at the base of the cantilever is the gate for a strain-sensing FET. The dark gray regions are etch trenches that define separate conduction channels for the two FETs, as illustrated in Fig. 5.4(b). The oval in Fig. 5.4(b) indicates the conduction channel for the charge-imaging FET. The strain-sensing FET channel lies at the cantilever base, where the strain from vertical deflections of the cantilever is maximum. This cantilever was fabricated from Wafer 960220C using the process illustrated in Fig. 5.2.

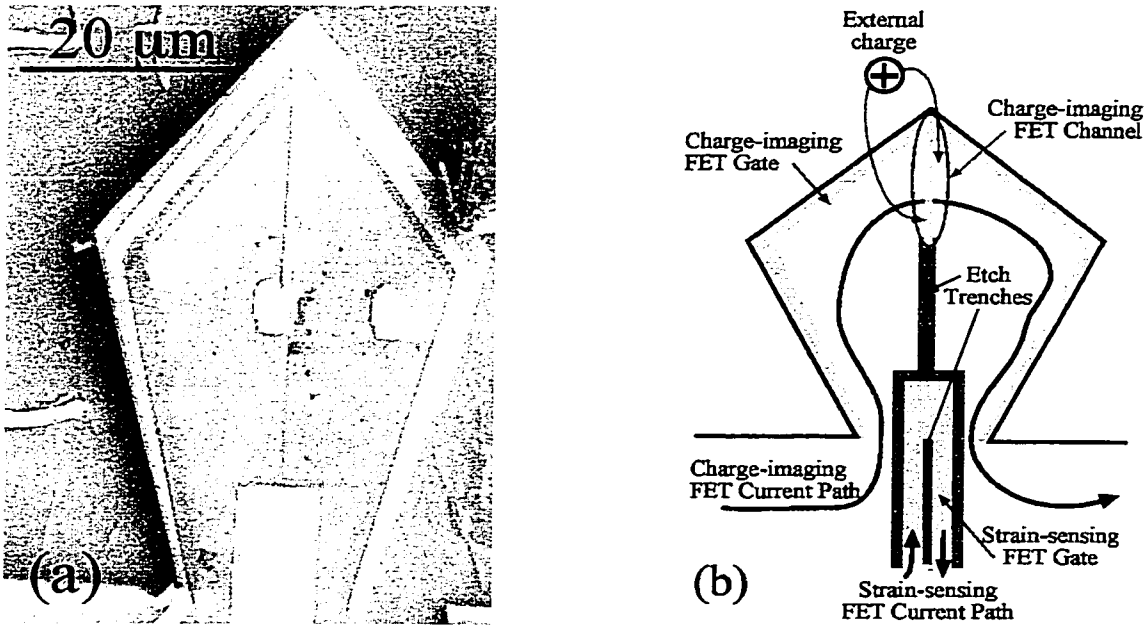

Figure 5.4 (a) Scanning electron microscope image of a cantilever with two integrated FETs. (b) Cantilever design. There is a third FET to be used as a switch in an area outside of the picture. For simplicity, the leads to the FET gates are not shown.

The FET at the top of the cantilever shown in Fig. 5.4 can be operated as a charge-imager using the circuit diagram shown in Fig. 5.5. First, the drain-to-source and gate-to-source voltages of the charge-imaging FET are set so the FET is in the current-saturation regime of its drain characteristics. Then, an FET switch (a third FET in an area outside of that shown in Fig. 5.4) is used to electrically disconnect the charge-imaging FET gate from the voltage source used to charge it. The existing charge on the gate keeps the charge-imaging FET in the current saturation regime, but now external charges can couple to the FET channel. The response to the external charge is a change in the drain current I_D. The charge-imaging FET gate was made symmetric to avoid twisting the cantilever, but this has the disadvantage of a large gate area, and consequently low spatial resolution when imaging charge.

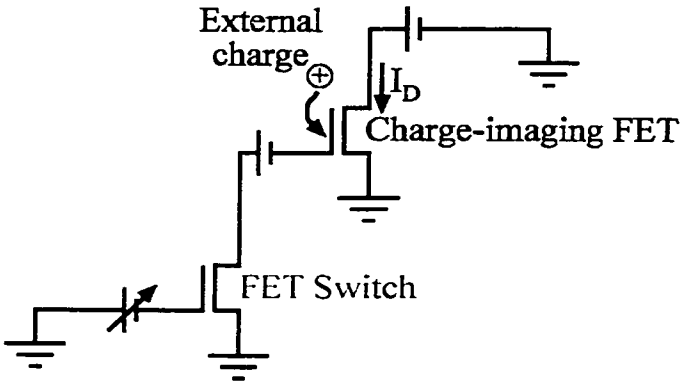

Figure 5.5 Circuit for operating the charge-imaging FET. The charge-imaging FET is set in the current saturation regime, and an FET switch is used to electrically disconnect the charge-imaging FET gate from the battery. This allows external charges to couple to the charge-imaging FET channel and change the drain current I_D.

Figure 5.6(a) is an SEM image of a charge-imaging cantilever with two integrated FETs. The bright, angled line that runs to the tip of the cantilever is the gate for a charge-imaging FET, and the bright rectangle at the base of the cantilever is the gate for a strain-sensing FET. The darker regions are etch trenches that define separate conduction

channels for the two FETs. The charge-imaging FET has a quantum point contact (QPC) geometry, and its channel lies at the cantilever tip, as shown by the oval in Fig. 5.6(b). This cantilever was fabricated from Wafer 990924B using the process illustrated in Fig. 5.3.

The FET at the tip of the cantilever shown in Fig. 5.6 responds to external charges near its channel by a change in its drain current, *c.f.* Chapter 4. The FET has a quantum point contact (QPC) geometry, and is operated in the current-saturation regime of its drain characteristics. The FET is kept in this regime with fixed drain-to-source and gate-to-source voltages, but because of its channel has a QPC geometry, it is still sensitive to external charges even when the gate is electrically connected to the voltage source used to charge it. This is no longer a need for an FET switch, and the QPC geometry gives the charge-imaging FET much improved spatial resolution over the design shown in Fig. 5.5.

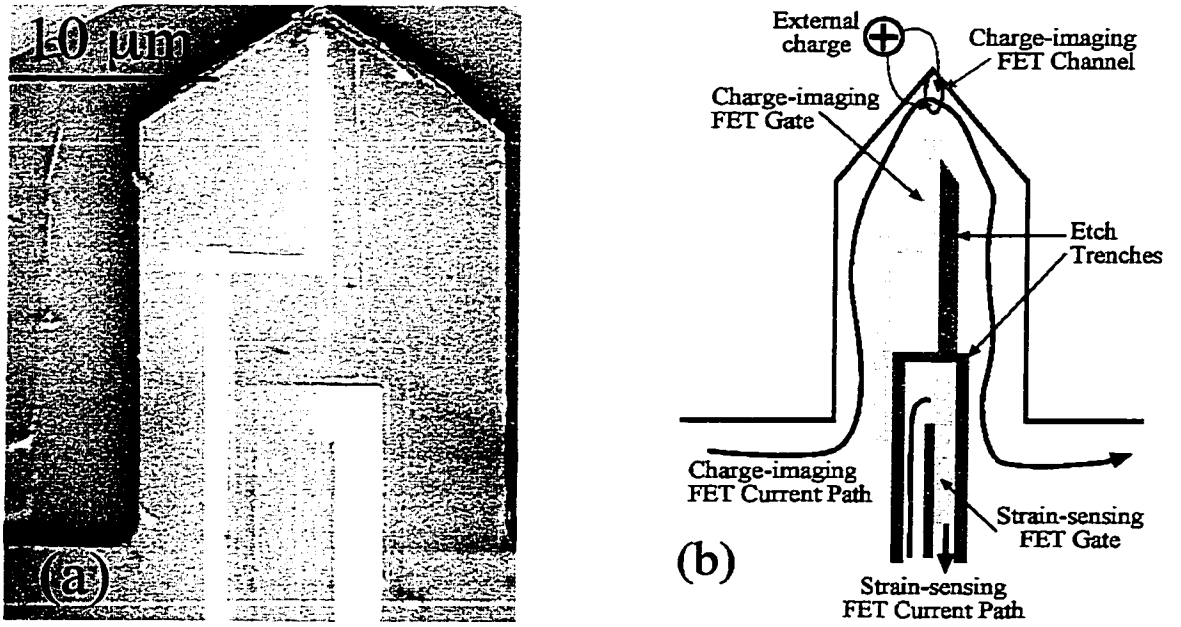

Figure 5.6 (a) Scanning electron microscope image of a cantilever with two integrated FETs. The FET at the tip has a quantum point contact geometry. (b) Cantilever design. For simplicity, the leads to the FET gates are not shown.

Section 5.3 Measurement Setups

The section describes measurements of the strain-sensing FET. Three measurements were performed: drain characteristics, noise spectrum, and response to mechanical excitations of the cantilever the FET is integrated on.

The drain characteristics of the strain-sensing FET were measured using the circuit shown in Fig. 4.6(b), with the strain-sensing FET in place of the charge-imaging FET. All voltages were referenced relative to the FET source ohmic contact. The low noise voltage source known as the "ramper box" (Katine 1996) was used to provide a smoothly increasing drain-to-source bias voltage V_{DS}. The bias voltage was increased until the drain current saturated, which typically occurred for $V_{DS} < +0.6$ V. The resulting signal from the source ohmic contact was amplified with an Ithaco 1211 Pre-amplifier. These measurement were taken for a series of gate-to-source voltages V_{GS}, which were taken separate output from the voltage source passed through a low-pass RC Filter with corner frequency 10 Hz. Both V_{DS} and I_D, the signal from the Ithaco Pre-amplifier, were measured using Fluke 8842A Digital Multi-Meters (DMMs). The data from the two DMMs was recorded using the apparatus described in (Beck 1998b).

The noise spectrum of the strain-sensing FET was measured using the circuit shown in Fig. 4.7(a), with the strain-sensing FET in place of the current-imaging FET. A low noise voltage source was used to provide the drain-to-source bias voltage V_{DS} and the gate-to-source voltage V_{GS}. The values of V_{DS} and V_{GS} were chosen so the strain-sensing FET is in the current-saturation regime of its drain characteristics. The drain current I_D was ac coupled to the Ithaco 1211 Pre-amplifier. The amplified signal from

the Ithaco 1211 was measured using an HP 3561A Spectrum Analyzer. The noise spectrum was recorded using the program described in (Mar 1994).

Figure 5.9 shows the setup used to detect the response of the strain-sensing FET to mechanical excitations of the cantilever the FET is integrated on. The cantilever is mounted above a piezoelectric bimorph sandwiched in between two copper ground places. The ground planes shielded the strain-sensing FET on the cantilever from the bimorph's electric fields. An HP 3325A Function Generator was used to excite the bimorph with a 0.5 V peak-to-peak amplitude sine wave with slowly increasing frequency. A dc voltage output from the signal generator was measured with a Fluke 8842A Digital Multi-Meter (DMM). The ac signal from the source contact was amplified using an Ithaco 1211 Pre-amplifier and fed into a PAR 124A lockin amplifier. The lockin amplified and integrated the signal at the frequency provided by the function generator, and the dc output was measured with a Fluke 8842A DMM. The data from the two DMMs was recorded using a Power Macintosh computer.

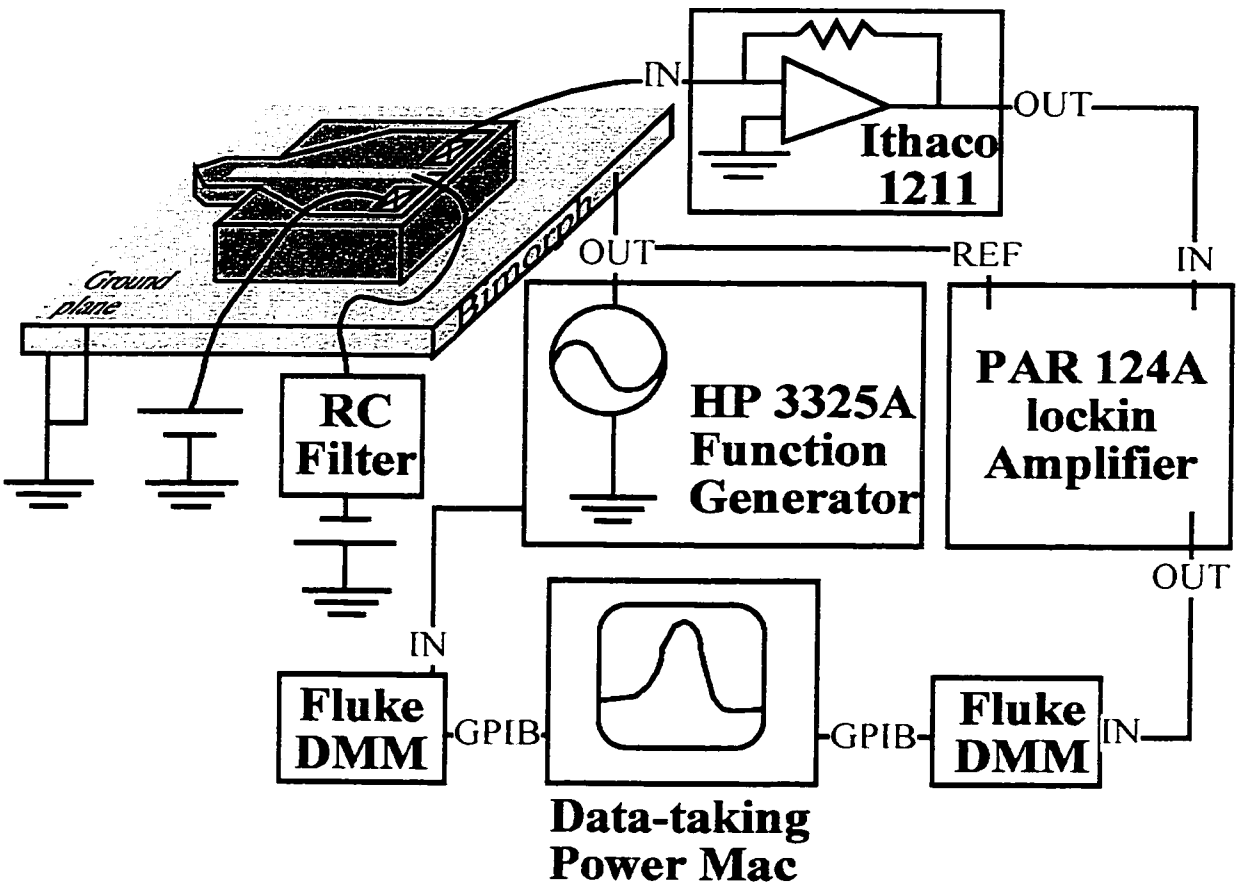

Figure 5.7 Setup for measuring the response of a strain-sensing FET integrated onto a cantilever. The cantilever sits on top of a piezoelectric bimorph which is electrically excited by a since wave with a slowly increasing frequency. The strain-sensing FET is biased in the current-saturation regime, and ac signal is amplified by an Ithaco 1211 Pre-amplifier and integrated by a PAR 124A lockin Amplifier.

Section 5.4 Drain Characteristics, Noise Spectrum, and Response to Mechanical Excitations

Figure 5.8 plots the drain characteristics of the strain-sensing FET at T = 4.2 K. The drain current I_D is measured as a function of the drain-source voltage V_{DS} for a series of gate-to-source voltages V_{GS}. The drain characteristics are those of a conventional FET – I_D saturates with increasing V_{DS} and in controlled by V_{GS}. For a typical operating point V_{DS} = +0.6 V, V_{GS} = -0.4 V, the transconductance g_m = 10 μS and the small-signal drain-to-source resistance r_{ds} = 45 MΩ.

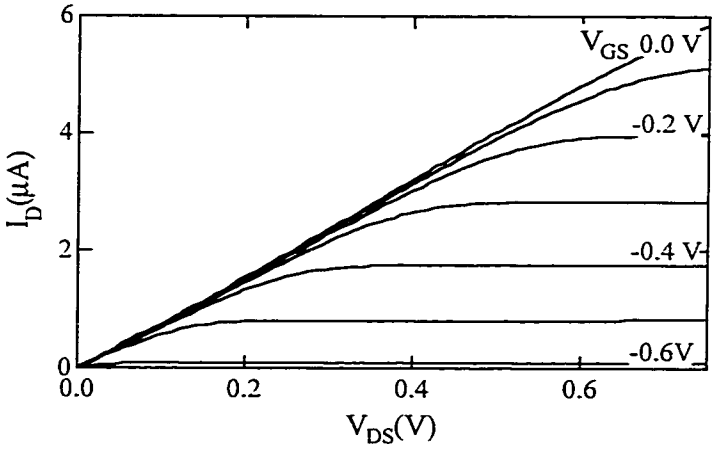

Figure 5.8 Drain characteristics of the strain-sensing FET at T = 4.2 K. The drain current I_D is plotted as a function of the drain-source voltage V_{DS} for a series of gate-to-source voltages V_{GS} spaced by –0.1 V. Some curves have been labeled with their gate-to-source voltage value. The drain current I_D saturates smoothly for V_{DS} < +0.75 V, a smaller voltage than most commercial FETs.

Figure 5.9 plots the gate voltage noise spectrum of the strain-sensing FET at T = 4.2 K. At low frequencies (< 1 kHz), the spectrum has a 1/f behavior, but it reaches the white noise level of v_n = 200 nV/Hz$^{1/2}$ at 10 kHz. The FET was voltage biased through its drain contact with drain-source voltage V_{DS} = +0.7 V, and the gate-to-source voltage was held fixed at V_{GS} = -0.375 V. The equivalent deflection noise level is

$z_n = 0.5$ nm/Hz$^{1/2}$ at 10 kHz. The deflection noise can be expressed in terms of the cantilever length L = 35 μm, the dielectric constant of $Al_{0.3}Ga_{0.7}As$ $\varepsilon = 12.54\ \varepsilon_0$ (Blakemore 1987), the heterostructure's Young's modulus E = 119 GN/m^2 (Blakemore 1987), the depth d = 52 nm thickness t = 20 nm of the 2DEG, and the piezoelectric constant of the heterostructure $d_{Het} = 3.03$ pC/N (Beck 1998b).

$$z_n = \frac{\varepsilon L^2}{3Edtd_{Het}} v_n \tag{5.1}$$

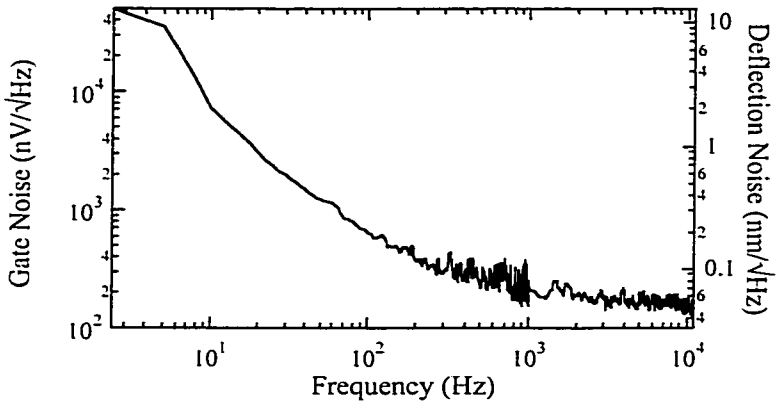

Figure 5.9 Noise spectrum of the strain-sensing FET. The drain-to-source bias voltage and gate-to-source voltage were set to V_{DS} = +0.7 V, V_{GS} = -0.375 V.

Figure 5.10 plots the of the drain current I_D of the strain-sensing FET integrated onto a free-standing cantilever. The AC response as a function of the mechanical excitation frequency of a cantilever has a sharp peak (Q ~ 600) at 159.8 kHz. The cantilever has length L = 35 μm, width w = 20 μm, and thickness h = 0.255 μm, as measured from Fig. 5.5(a). The heterostructure (Wafer 960220C) has Young's modulus E = 119 GN/m^2 and density ρ = 5084 kg/m^3 (Blakemore 1987). Equation 2.15 provides an estimate for the cantilever resonant frequency f_{res} = 162 kHz, in good agreement with

the measured value. The strain-sensing FET was biased in the current-saturation regime with V_{DS} = +0.6 V, V_{GS} = -0.45 V. The cantilever is fabricated using the process illustrated in Fig. 5.2.

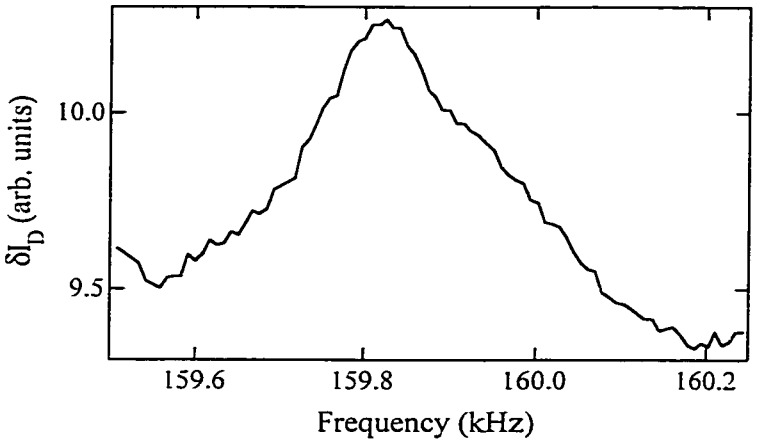

Figure 5.10 Change in drain current δI_D as a function of bimorph excitation frequency.

Section 5.5 Summary

In conclusion, we have fabricated cantilevers with integrated FETs which can be used for simultaneous charge-imaging and strain-sensing. The cantilevers were fabricated from a GaAs/AlGaAs heterostructure in a series of aligned electron-beam lithography steps, and a hydrofluoric acid etch to free the cantilever. and and arrays of cantilevers have been fabricated. At liquid He temperatures, the measured drain characteristics of the strain-sensing FET show the drain current I_D saturates smoothly with increased V_{DS} and is controlled by the gate-to-source voltage V_{GS}. The strain-sensing FET has a deflection noise level < 1 nm/Hz$^{1/2}$ at 10 kHz.

Chapter 6 Conclusions

This thesis has described experiments which investigated how to create a highly sensitive, moveable charge sensor using a field-effect transistor at the end of a scanned probe microscopy cantilever. Such sensors would allow direct imaging of electron flow through nanostructures.

Chapter 4 described measurements of a charge-imaging field-effect transistor (FET) fabricated with a quantum point contact (QPC) geometry to achieve high spatial resolution and excellent charge sensitivity. The FET charge response is confined to a disc with full width at half-maximum (340 nm) comparable to its channel width (250 nm). The FET charge noise spectrum reaches values « 1 $e/Hz^{1/2}$ at 30 kHz. The FET was fabricated in a GaAs/$Al_xGa_{1-x}As$ heterostructure designed for making scanned probe microscopy (SPM) cantilevers. Thus, a moveable charge sensor can be easily made by integrating the FET onto a SPM cantilever.

Chapter 5 described SPM cantilevers with integrated FETs that have been fabricated from a GaAs/$Al_xGa_{1-x}As$ heterostructure. A strain-sensing FET integrated at the cantilever base functioned as a deflection sensor. A response peak in the drain current of the FET was measured when the cantilever was mechanically excited at its resonant frequency.

Possible future experiments include demonstrating the charge-imaging FET's sensitivity to single electrons, creating a charge- and topography-imaging cantilever, and directly measuring the electron distributions in nanostructures. The magnitude of the charge response and the noise levels measured in Chapter 4 indicated the FET will be

sensitive to single electrons. Fabricating a quantum dot next to the charge-imaging FET is the clearest way to demonstrate the FET's charge sensitivity. The charge of a quantum dot can be changed one electron at a time, making it a natural system to use for calibration. A scanning electron microscope (SEM) image of this device showing this is shown in Fig. 6.1(a). The dark regions are etch trenches, and the bright features are electrostatic gates. Two charge-imaging FETs are formed on the left side of the vertical etch trench, and two quantum dots are formed on the right side of the etch trench. A schematic is shown in Fig. 6.1(b). Power gain is achieved by biasing an FET in the current-saturated regime instead of a point contact in the tunneling regime (*c.f.* Field 1993).

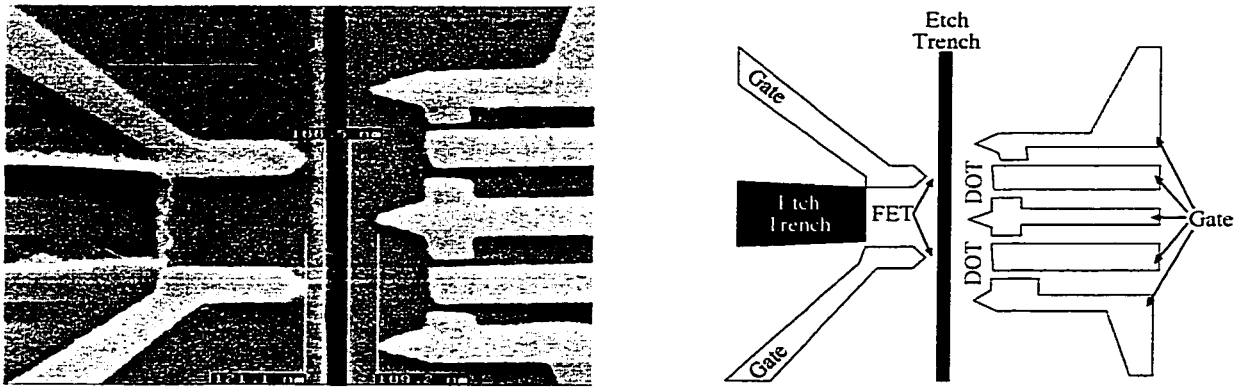

Figure 6.1 (a) Scanning electron microscope image of a charge-imaging FET next to a quantum dot. The dot can be used to demonstrate the FET's sensitivity to single electrons. (b) Schematic illustrating the device.

A simultaneous charge-imaging and topography-mapping sensor can be made from an SPM cantilever with two integrated FETs. Charge-imaging is achieved with an FET with a QPC geometry can be formed right at the tip of the cantilever. Topography-mapping is achieved with a strain-sensing FET formed at the cantilever base, where the strain resulting from deflection is maximal.

Finally, creating an array of charge-imaging and topography-mapping SPM cantilevers would greatly improve the scanning speed and area (*c.f.* Minne 1998a, Minne 1998b). Figure 6.2 shows an SEM image of four free-standing cantilevers of a ten cantilever array. The dark areas underneath the cantilevers is the air gap between the cantilever and the underlying substrate. Fabricating an array follows the same process as fabricating a single cantilevers. The only additional difficulty is more care has to be taken to creating separate current paths for FETs integrated onto the cantilevers.

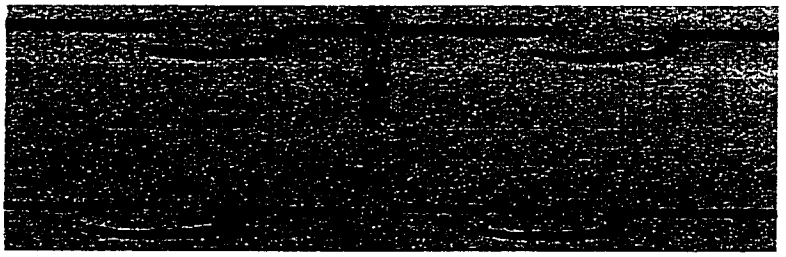

Figure 6.2 Array of four free-standing cantilevers of a ten cantilever array fabricated from the heterostructure denoted Wafer 990924B. The dark areas underneath the cantilevers are air gaps between the cantilevers and the substrate.

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Appendix A Fabrication Equipment Procedures

Section A.1 Cleaving GaAs Chips

This section describes the procedure for cleaving mm × mm size chips from a 3" diameter heterostructure wafer. The wafers are normally stored in a nitrogen "dry box", which is maintained at a slight overpressure with boil-off gas from a liquid nitrogen storage dewar. A dust/particle filter mask should be worn to avoid breathing in GaAs dust when cleaving.

1. Remove the wafer from the dry box and insure that you know which side is up.[18] One way to tell is to look at both surfaces of the wafer next to a GaAs chip. In the optical microscope, the GaAs and back sides of the wafer will look white. The side with the two-dimensional electron gas (2DEG) underneath will look a slightly different color due to the heterostructure layers.
2. Once you have determined which side has the 2DEG, scribe "X"s on the other side using the diamond-tipped pencil.
3. Spray the chip with methanol (D&I – Item #M-371-008), and blow dry the chip with ultra-high purity nitrogen gas (UHP N_2).
4. Scribe a cleave line with the diamond-tipped pencil.
5. Clean with methanol as in Step 3, and place the wafer on a Teflon-covered microscope slide, with the scribe line over the edge of the slide.
6. Hold the wafer to the slide with a piece of folded filter paper. Then, gently press down on the other side with another piece of folded filter paper until the wafer cleaves along the scribe line.
7. Clean both pieces with methanol as in Step 3.
8. If not done already, use the technique described in Steps 4-7 to cleave the wafer into quarter-wafers, as shown in Fig. A.1(a).
9. Take a quarter-wafer and cleave a long rectangle of the desired width, as shown in Fig. A.1(b).
10. Next, cleave off chips of the desired length as shown in Fig. A.1(c). Store the chips in anti-static sample holder, and return the remaining heterostructure to the nitrogen "dry box".

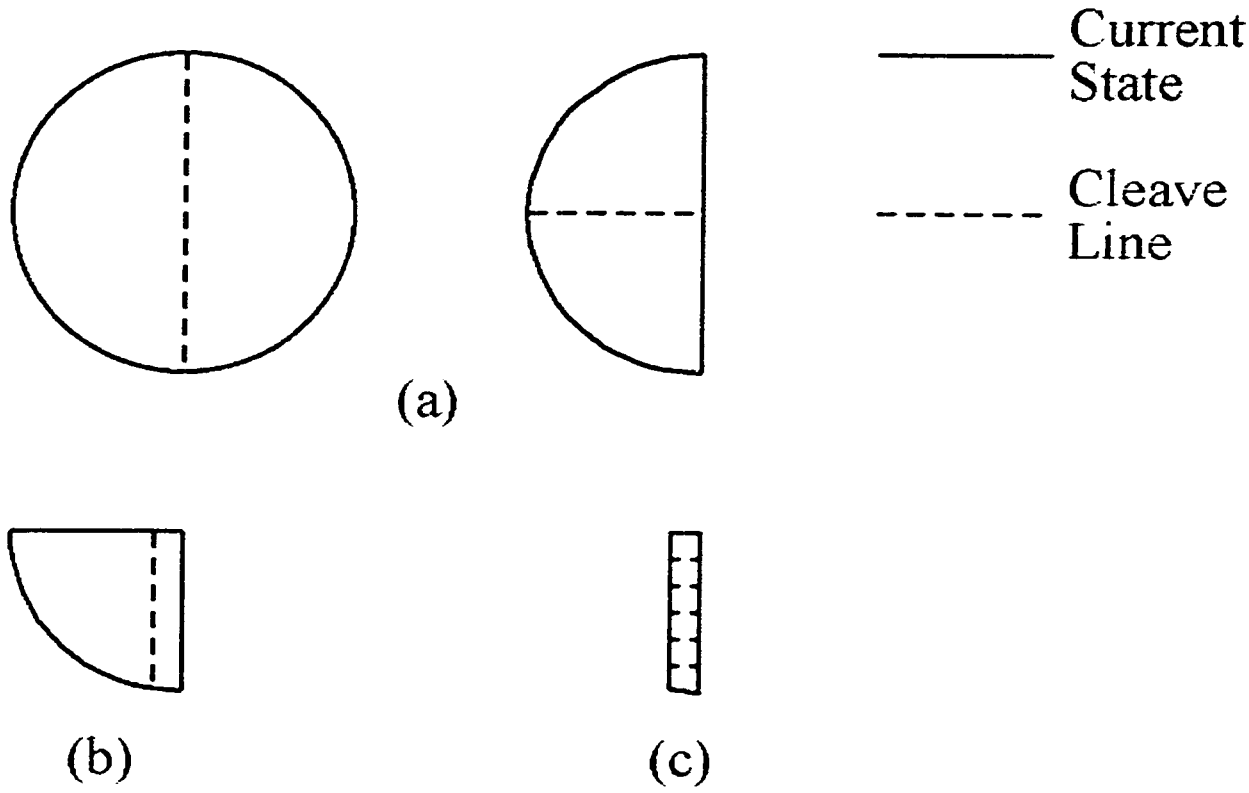

Figure A.1 Process for cleaving a 3" diameter heterostructure wafer into (a) quarter-wafers (b) mm-wide strips (c) mm × mm size chips.

[18] Otherwise, you may painstakingly go through an entire fabrication run and then realize that it has all been for naught as the 2DEG is on the other side. This is very demoralizing.

Section A.2 Spinning Resist

This section describes the procedure for applying, or spinning, polymethylmethacrylate (PMMA) resist onto millimeter-sized chips to prepare them for electron-beam lithography (Appendix A.3). This process consists of two steps: cleaning the chips in a series of organic solvents and spinning PMMA onto the clean chips.

Subsection A.2.1 Cleaning the chips

1. Pour trichloroethylene (TCE) into the glass beaker dedicated for cleaning with TCE until the TCE level is 2 to 3" from the bottom.
2. In the fume hood, heat the beaker on a hot plate set to 150°C.
3. Place the chips into Teflon beakers, ideally one chip per beaker. The Teflon beakers protect the chips from being shattered by contact with the glass beakers. If there are many chips, it is acceptable to put two in a single Teflon beaker, but one must take care to place them on opposite sides of a Teflon beaker, so one chip does not scratch the other's surface.
4. Place the Teflon beakers into the TCE, and then cover the beaker securely with aluminum foil labeled, "HOT TCE". Press the aluminum foil to form a tight seal with the lip of the beaker to minimize the amount of evaporating TCE that escapes into the fume hood, and thus the atmosphere.
5. While the TCE boils, pour acetone into the glass beaker dedicated for acetone, as in Step 1.
6. After 10 minutes, transfer the Teflon beakers from TCE to acetone.
7. Some of the next steps depend on whether there are fine, deposited features, *e.g.* gates but not etch trenches, on the chip or not. If there are, then follow the steps labeled (i), and if there are not, then follow the steps labeled (ii).
8. (i) Let them sit in the beaker for 10 minutes. (ii) Place the beaker into the ultrasound cleaner and sonicate it for 10 minutes.
9. Take the beaker, an anti-static sample box (FWI – Item #H20-426-62C02, H20–02–62C02), and a set of tweezers into the inner clean room.[19]
10. Locate a glass beaker dedicated for methanol and pour in methanol, as in Step 1.
11. (i) Transfer the Teflon beakers from acetone to methanol. (ii) Let them sit in the beaker for 5 minutes
12. Place the beaker into the ultrasound cleaner and sonicate it for 5 minutes.
13. While waiting, complete Steps 14-20 below.
14. Place a new cleanroom wipe on the solid part of the counter in the flow hood.
15. Take an airgun from its clip and place it on the counter within easy reach.

[19] Along the way, remember to get the key to the inner lceanroom lockbox, which holds the PMMA. This key is located in the outer cleanroom lockbox.

16. Keeping track of which side is up, gently remove a chip from methanol and place it facing up on the cleanroom wipe, gripping it firmly with your tweezers.
17. As you place the chip onto the wipe, take the airgun with your free hand and blow all the methanol off both the chip and especially the tweezers. Once you start blowing, do not stop until all the methanol is gone, especially on the tweezers, so none drips back down onto the chip and leaves a film.
18. Place the chip into a anti-static container.
19. Repeat Steps 16-17 for all the other chips, one at a time.

Subsection A.2.2 Spinning

20. Set the target temperature of a hot plate to 180 °C.[20]
21. Turn the spinner on, and set the time for "SPEED 1" to 5 s and the time for "SPEED 2" to 60 s.
22. The spinner has a safety interlock that prevents it from spinning unless sufficient vacuum is drawn through the spinner hole. If the vacuum lines become clogged with resist, this interlock is fooled and allows unwanted starts of the spinner. This can result in the horrifying view of one's prized sample flying off the chuck. To prevent this tragedy, one should first test the vacuum line by stepping on the foot pedal to activate the spinner. The spinner should buzz, but not spin. If it does start spinning, spray acetone down the vacuum line until enough resist has been dissolved that the interlock becomes functional and stops the spinner.
23. Make sure all the holes of the spinner chuck are clear, cleaning out old resist, if necessary.
24. Mount the chuck onto and place the drip bowl around the spinner.
25. Test the spinner again, as in Step 22.
26. Press a small piece of Al-foil over the top chuck hole.
27. Start the spinner with the foot pedal, and use the potentiometer dials to set "SPEED 1" to 500 rpm and "SPEED 2" to the appropriate value shown in Table A.1.
28. Use the second set of potentiometer dials to set the acceleration so full speed is reached within 1 s.
29. Set the spinner on "SPEED 2" mode.
30. Clean an appropriate number (one for each different type of PMMA and new ones for each layer) of glass pipettes. This is done by spraying a small amount of methanol into it, and blowing air through the pipette tip to dry it. After cleaning, make sure nothing touches the pipette tip; so, it does not contaminate the PMMA.
31. Take an equal number of rubber bulbs and blow out the dust inside with the air gun.
32. Place a chip over the hole on the chuck, aligning its center with the hole's.
33. Draw the appropriate PMMA solution into the glass pipette and clear out the air bubbles. Then, carefully put one drop on the center of the chip and start the spinner immediately with the foot pedal.
34. After the spinner stops, use metal tweezers to place the chip onto the hot plate.
35. Repeat Steps 32-34 for each chip.

[20] It is faster to the hot plate to 222°C, then switch to 180°C after a few minutes.

36. Set the spinner to "SPEED 1 AND 2" mode. The spinner will now spin at Speed 1 for 5 s before automatically ramping up to Speed 2.
37. Start the chip spinning at Speed 1, and pipette PMMA onto it while it is still spinning. Then let it automatically ramp up to Speed 2 and spin at the higher speed for 60 s.
38. After all the layers have been spun onto all the chips, clean the spinner chuck and bowl with first the acetone and then the methanol you used to clean the chips. Wipe the bowl with a cleanroom wipe after each solvent, and pick out any resist that maybe stuck in the chuck.
39. Turn the hot plate and spinner off and exit the cleanroom.

Notes: It is of course, better to do several chips at once because of the fixed time overhead (TCE/acetone/methanol cleaning, etc...). This section describes spinning the ships around the same axis as the spinner. Sometimes it is desirable to spin the chips using the off-axis spinner chuck (Beck 1998b) known as the Favalora Device Mark III.

Fabrication Step	1st layer (PMMA type/speed)	2nd layer (PMMA type/speed)	3rd layer (PMMA type/speed)
Ni:Au:Ge ohmic contacts	4% 496K / 5 krpm	2% 950K / 5 krpm	2% 950K / 5 krpm
Cr:Au electrostatic gates	6% 496K / 5 krpm	2% 950K / 5 krpm	N/A
Shallow etch (≤ 60s ion mill)	4% 950K / 5 krpm	4% 950K / 5 krpm	N/A
Deep etch (60 to 100 s ion mill)	4% 950K / 3.5 krpm	4% 950K / 3.5 krpm	N/A

Table A.1 PMMA resist types and spinning speeds for different fabrication steps.

Section A.3 Electron-beam lithography

This section describes the procedure for using the JEOL scanning electron microscope (SEM) for electron-beam lithography, starting from mounting the chip on an SEM sample mount, and ending with removing the written sample from the SEM.

Subsection A.3.1 Mounting the Chip

Figure A.2(a) shows the sample mount for loading chips into the SEM. The sample mount is a 1 cm tall, 1.25 cm diameter aluminum[21] cylinder[22] with a small (~ 1 mm diameter) hole drilled into it to aid in measuring the SEM beam current.

1. Wearing gloves, clean all surfaces of the sample mount with isopropyl alcohol (IPA) and a wiping cloth (TX 609 TechniWipes – available in the chemistry stockroom).
2. Firmly hold the chip to be mounted with a pair of plastic tweezers[23]. Gently scrape off any residual PMMA off the back side of the chip with a clean scalpel.
3. Place the chip on the top surface (one with drilled hole) of the mount so the drilled hole is to the left of the left side of the chip.
4. Take a wooden applicator stick and break it so that there is an flat, angled face at the end like the ones shown in Fig. A.2(b).[24] Then make another.
5. Take one applicator stick, and touch the angled tip to the carbon paint (SPI – Item #5006) brush. The carbon paint should be thick, but not congealed. If necessary, add thinner (SPI – Item # 5007) to get the carbon paint of the desired viscosity.
6. Bring the angled tip close to the one side of the chip, but place it on the surface of the mount before it touches the side of the chip. Then, slowly push the carbon paint until it just touches the side edge of the chip. Carefully remove the applicator before the carbon paint dries and attaches the stick to the chip. Quickly repeat on the opposite side of the chip. Otherwise, the drying carbon paint will pull one side of the chip off the surface.

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[21] It is important to use aluminum for the mount material as copper, another common mount material, diffuses extremely well into GaAs. Any Cu that diffuses into the heterostructure will add unwanted donor sites and lead to noisier devices.

[22] If making a new mount, it is important to insure that the surfaces are flat. This is done by milling the surfaces and moving them in a figure-eight pattern over a sheet of sandpaper on a level granite slab. For assistance, contact Stan Cotreau, the student machine shop manager. Remember to ask nicely and politely.

[23] Using metal tweezers runs the risk of shattering the chip with too much applied pressure.

[24] As it can take many tries to make a good tip, once you make one you like, store and reuse it.

7. While the carbon paint is drying (~ 2 minutes) shake the silver paint (SPI – Item # 5001) bottle and coat the angled end of the second applicator stick with silver paint. Set the stick on a clean piece of filter paper to dry.
8. Once the carbon and silver paint are dry, hold the mount by the sides and use the 10×–40× microscope to focus on the top surface of the chip. Take the applicator stick with silver paint, and gently brush the top corners[25] of the chip without scratching the PMMA. The goal is to leave flecks of silver paint on the chip for focusing the SEM beam.

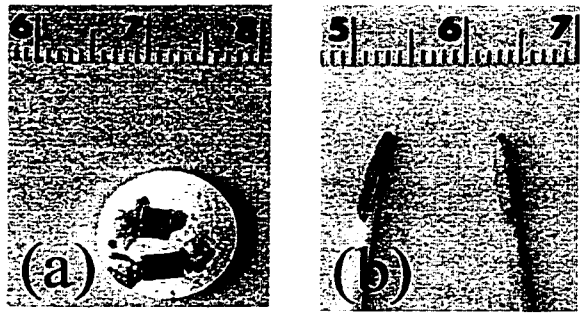

Figure A.2 Tools for preparing chips for electron-beam lithography. (a) GaAs/AlGaAs chips mounted on JEOL SEM sample mount. (b) Wooden applicator sticks used to apply carbon and silver paint when mounting the sample. The length scale in both figures is in cm.

Subsection A.3.2 Loading into the JEOL SEM

9. Place the mount in the sample holder so the set screw is to the left of the chip. Rotate the mount so that edges of the chip are parallel to the edges of the sample holder, as shown for the top chip in Fig. A.3.
10. Adjust the set screw on the bottom of the sample holder so the top surface of the chip is level with the top surface of the sample holder.
11. Screw the sample holder onto the loading stick, and push the plastic disc on the loading stick towards the sample holder.
12. Check the stage fine Z-adjustment is "0", and the rotation adjustment is set to "000".
13. Without anything touching the chip, place the sample holder inside the airlock, pressing the plastic disc against the O-ring at the airlock mouth.
14. Press the lit, red button above and to the right of the airlock to evacuate the airlock. The normal chamber pressure is ~ 0.5 μT. While the airlock is being evacuated, it will rise to ~ 0.5 mT.
15. When the light goes off, there should be a "whoosh" sound indicating the airlock has been pumped out. Turn the cylindrical gate handle to the right of the airlock towards the front of the airlock, *i.e.* counter-clockwise (CCW) if looking down the handle

[25] Alternatively, one can leave flecks of silver paint as close to the area where the finest features are to be written. This leads to better focusing than averaging from the corners, but runs the risk of putting silver paint where it is not wanted.

axis, as far as it will go. Then, pull the gate handle to the right, opening the gate. Once the gate is fully open, turn the handle away from you, *i.e.* clockwise (CW) looking down the handle axis, so the gate does not slide back to the closed position.

16. Push in the loading stick until the sample holder mates with the stage. Make sure they are truly locked together[26] by trying to tip the sample holder upward gently using the handle of the loading stick.
17. While pushing on the loading stick handle, unscrew the loading stick from the sample mount holder.
18. While pushing on the plastic disc on the loading stick, pull the loading stick handle outward until the loading stick is clear of the gate.
19. Close the gate by reversing the procedure described in Step 15.
20. The chamber pressure should drop quickly from ~ 0.5 mT to ~ 30 μT. Otherwise the gate is not closed.
21. Press the red button above and to the right of the airlock to vent the airlock.
22. After 5 s, the airlock should be vented. Remove the loading stick and lay it aside.

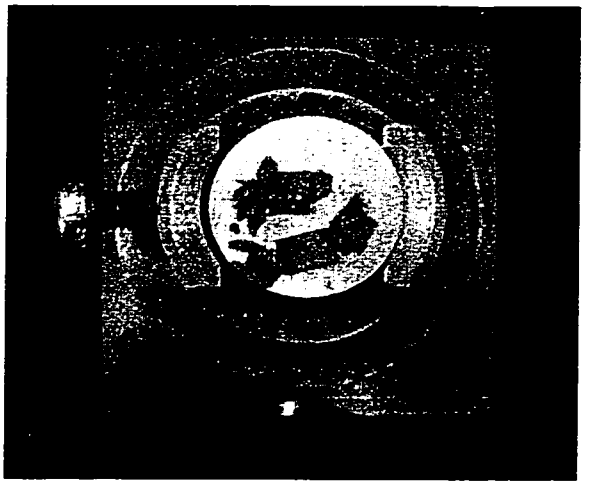

Figure A.3 Mounted chip inside sample mount holder for JEOL SEM. The set screw on the left hold the sample mount in place, and another on the bottom raises and lowers the sample mount.

[26] If the sample holder falls off the stage, then the SEM chamber has to be opened up, cleaned, and pumped back down to low pressures. This is a not fun. Avoid it.

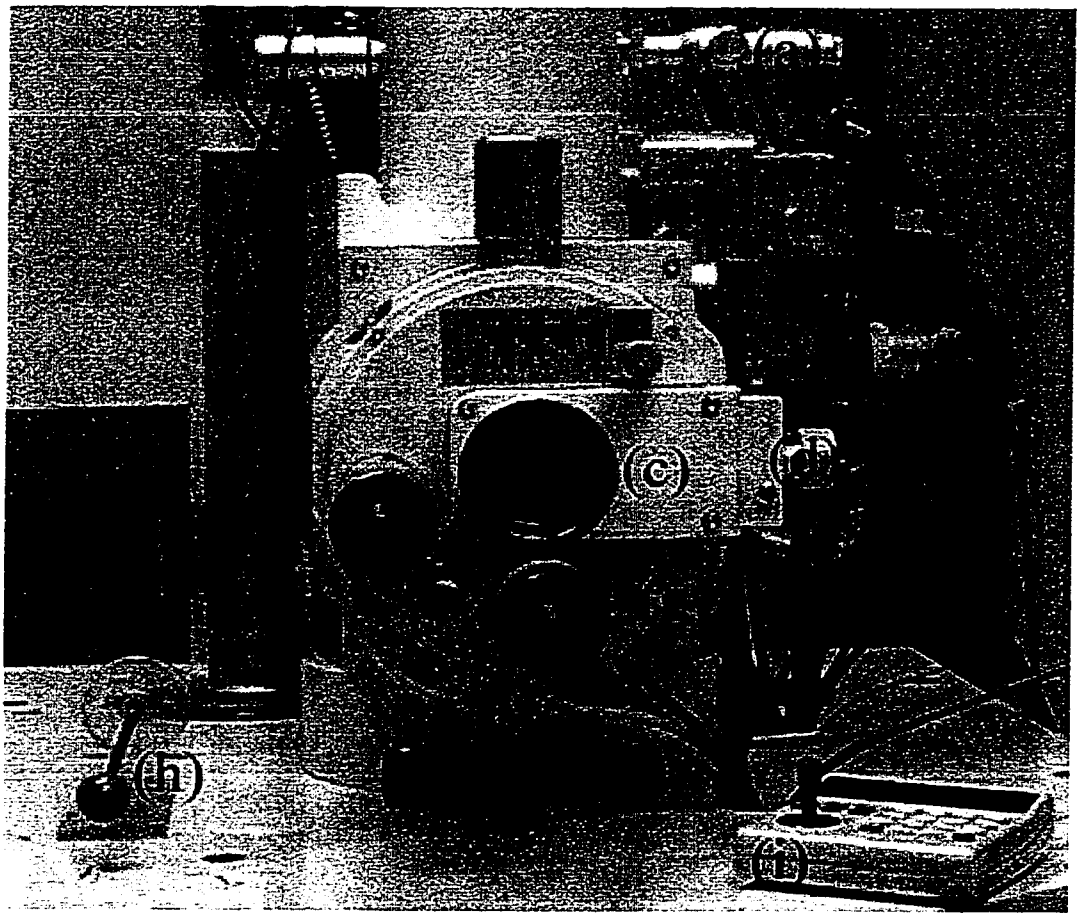

Figure A.4 Main body of the JEOL scanning electron microscope. Labeled features are (a) Wobble Adjustment (b) Rough Z-Adjustment (c) Airlock (at left) (d) Gate Handle (e) Liquid Nitrogen Fill Can (f) Fine Z-Adjustment (g) Stage Rotation Control (h) Loading Stick (i) Stage Control Panel.

Subsection A.3.3 Saturating the Filament

This subsection describes getting the maximum, stable filament current. The SEM is computer-controlled, and "keys" refer to those on the SEM control keyboard (Fig. A.6) "Selecting" a mode on the SEM refers to using the arrow keys to highlight the mode and pressing the "ENTER" key to select it. There is a secondary control panel for the SEM, and all "knobs" and "lighted buttons" are on this panel. The stage is also computer-controlled, and "buttons" are those on the stage control keypad (Fig. A.5) Setting the

coarse condenser lens value by turning the "PROBE CURRENT" knob will be denoted as "Set CL = value". CW and CCW refer to the orientation when looking down the axis of a knob.

23. Move the stage 6.1 mm to the right[27] so the PMMA is not exposed while adjusting the filament current.
24. Set the beam-to-stage working distance to 15 mm by turning the rough Z-adjustment until the "15" setting is locked in.
25. Fill the liquid N_2 fill can for the cold trap of the diffusion pump.
26. Press the "MEMO" or "PF5" key on the SEM control keyboard.
27. Use the arrow keys to highlight "ACC35 WD15", and press the "L" key to load the parameter file for accelerating voltage 35 kV and working distance 15 mm. If the selection cursor is on the left-hand monitor, then press the "ESC" key to bring it back to the right-hand monitor.
28. Press the "PF2" key, and then the "1" key. Use the "CONTRAST" and "BRIGHTNESS" knobs to set both parameters to 200.
29. Set CL = 12.
30. Press the "2" key, and use the arrow keys to highlight "SEM" and press "ENTER" to select that operation mode. "SEM" should then be flanked by outward pointing arrows, which will look like "◁ SEM ▷".
31. Select "LSP".
32. Press the "FAST" button to select a fast scan speed.
33. Set the "IMAGE" and "POSITION" shifts to (X, Y) = (0, 0) by using the "IMAGE/POSISITON SHIFT" knobs on the SEM control panel and the "POSN" button to toggle between which of the two you are changing.
34. Press the "3" key and then turn the accelerating voltage on by pressing the "ON" button. If the "SEI" mode is not automatically selected, manually select it.
35. The filament current behaves as shown in Fig A.8. It peaks, falls, peaks again, and then plateaus. The optimal operating point is just below the plateau, and the current is measured by the amplitude of the line scan on the left screen. To find the operating point, slowly turn the filament knob CW until the current plateaus, then turn the knob CCW slightly. A good turning speed is halfway between two marks ("1/2 o'clock") every 5 seconds. The filament gauge reads ~240 μA with a new filament and ~180 μA when the filament is about to burn out.
36. Sometimes, the current does not plateau, but decreases as the knob is turned CW. In this case, go 1/2 o'clock past the point where the current begins to decrease, maximize the current as described below in Steps 37-39, find the shoulder again, and repeat Steps 37-39.
37. Press "1" to return to the first screen. Set CL = 12. With the "TILT/SHIFT" button dark (push and release to switch between light and dark), and adjust the tilt (beam

[27] To move (X mm, Y mm) relative to the current position, press the "GO REL" button on the stage control, then enter "X, Y, 0", pressing the "ENTER" button after each number.

angle relative to plane of sample) using the "X" and "Y" knobs to maximize the amplitude of the signal on the left screen.

38. Set CL = 4, push the "TILT/SHIFT" button (it should be lit), and adjust the shift (beam location relative to the sample) using "X" and "Y" knobs to maximize the amplitude of the signal on the left screen.
39. Press the "TILT/SHIFT" button again so the "X" and "Y" knobs are back on "TILT" mode and iterate Steps 37-38 until the signal amplitude is maximum.
40. The filament is now saturated. Set CL = 16, and press the "PIC" button to set the left screen on imaging mode. One should see the left edge of the circular sample mount.
41. Fill the liquid N_2 fill can for the cold trap of the diffusion pump again.
42. Press the "LENS CLEAR" or "PF10" key to degauss the electric plates that control the X-Y position of the beam.
43. Move the stage with the stage control joystick so the hole in the sample mount is in the center of the screen. Zoom in to magnification 1000× so the entire field of view is contained within the hole. Flip the current measurement switch from "ALARM" to "AEM" mode, and measure the beam current in the ammeter.
44. Adjust the fine condenser lens setting until the beam current is 3.0 pA.

Figure A.5 Control panel for motorized stage. The "<" and ">" symbols have been overlaid over the speed buttons to indicate which buttons decrease and increase the stage movement speed, respectively.

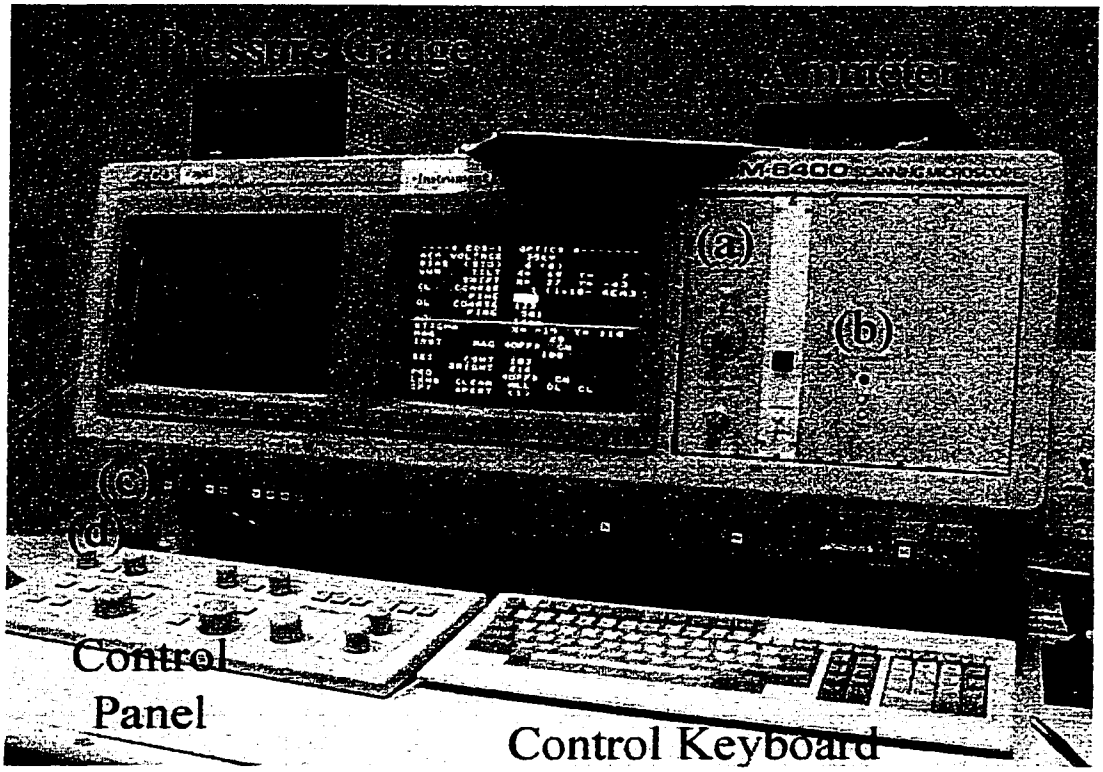

Figure A.6 Control keyboard, panel, and monitors for the JEOL SEM. Labeled controls are (a) Scan Rotation (b) Beam Blanking (c) Wobble (d) Pomona Box to Switch to Computer Control (e) Accelerating Voltage (f) Tilt/Shift (g) Filament Knob.

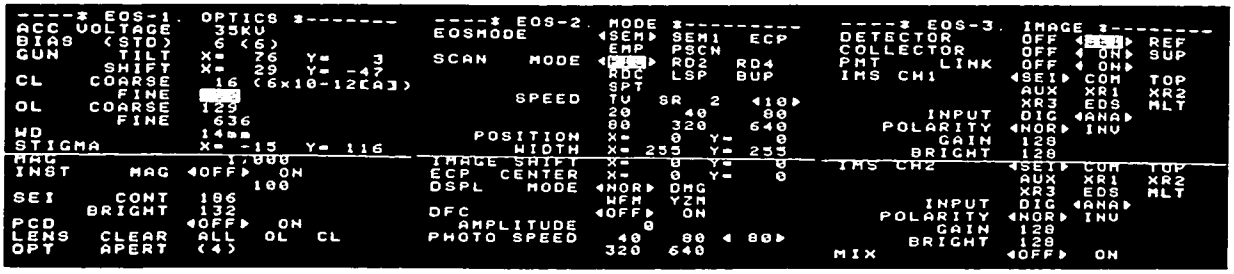

Figure A.7 First, second, and third screens (l-r) of SEM control program.

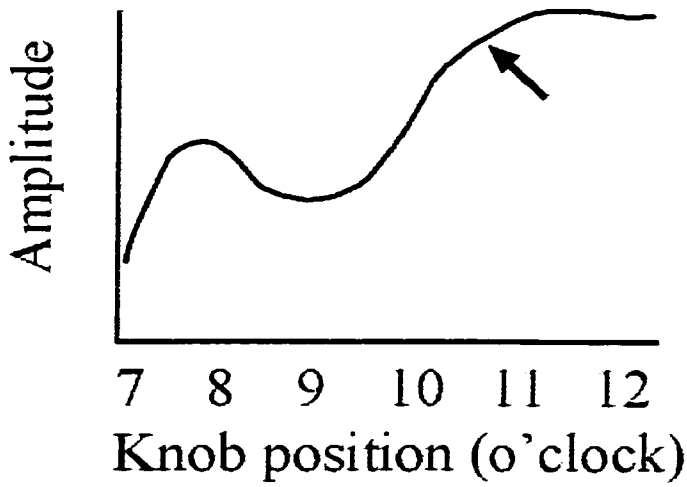

Figure A.8 Filament current as a function of filament knob position. The arrow indicates the desired operating point.

Subsection A.3.4 Focusing the Beam

This subsection describes how to set the rotation of the beam and sample, and how to position the sample so consecutive lithography steps are aligned to each other.

45. Check that the magnification and scale bar are displayed on the left screen. If they are not, press "ESC" to move the cursor from the right to the left screen. Press "BREAK" to display the scale bar, and press "ESC" again to move the cursor back to the right screen.
46. Press "2" and select the "BUP" setting to overlay cross-hairs over the image.
47. Use the "MAGNIFICATION" knob to set the magnification to 100×, and look for the hole drilled in the sample mount.
48. Use the stage control joystick to position the sample mount so the horizontal cross-hair (X-line) is tangent to the bottom of the hole.
49. Turn on the "SCAN ROTATION" switch, and use the "SCAN ROTATION" dial to adjust the image until the bottom of the hole remains tangent to the X-line as you move the sample back and forth horizontally. A typical setting is a few degrees CW.
50. Zoom out to magnification 20×, and move the stage so the left edge of the chip appears on the screen. Use the stage rotation knob to adjust the image until the left edge runs roughly vertically. Zoom in to magnification 650× and place the top left corner of the chip in the cross-hairs. Use the "FOCUS" knob to bring the corner into focus.

51. The top and bottom left corners of the chip should line up when we move the stage vertically. To adjust the rotational alignment, place one corner in the cross-hairs, move vertically, and use the stage rotation knob to adjust the chip so the corner is halfway to the vertical cross-hair. Reposition this corner in the cross-hair, move vertically the other direction, and bisect the new angle. Iterate this process, as illustrated in Fig. A.9, until both corners fall in the cross-hairs when the stage is moved vertically. The chip is now coarsely rotationally aligned.
52. The next step is to focus the beam. Move to the top left corner, and select the "PIC" mode. Turn the contrast to maximum (255) and adjust the brightness for the image clearest. Zoom in to magnification 500× and use the "FOCUS" knob to focus on one of the silver paint flecks. Keep zooming and focusing[28] until the silver paint is in focus at magnification 100,000×, and write down the focus settings.
53. The "FOCUS" knob adjusts the focal plane, but the beam may have an elliptical cross-section, which will blur the pattern features. The "STIGMATOR" knobs adjust the beam profile. Turn the X stigmator knob until the image looks blurry. Then, turn it back the other direction until the image is sharp again. Repeat for the Y stigmator knob, and iterate between the X and Y knobs until the image does not get any sharper.
54. Press the "WOBBLE" button. Adjust the wobble adjustment knobs until the image is stationary and only moves in and out of focus. Then, press the "WOBBLE" button again.
55. Zoom out to magnification 200×, move to the top right corner, and repeat the focusing procedure (Step 52) but not the stigmation adjustment. Write down the focus settings.
56. Enter the average[29] of the focus setting values from the two corners into the control program.
57. Zoom out to magnification 200×, and measure the beam currents (Steps 42-43) at the condenser lens settings to be used in writing the pattern.
58. Set CL = 16, and enter the measured beam current values into the parameter run file[30].

---

[28] It's best to focus on a fleck that has a curved edge as straight edges can look straight even when out of focus.

[29] One can also measure the distance between the two corners and the center of the pattern to be written and use a linear interpolation to more exactly determine the focus at the center of pattern. However, as the fine features are usually close to the center, it's generally sufficient to take a simple average.

[30] The run files have the "..rf6" suffix, and are accessed via the command "mrf name.rf6".

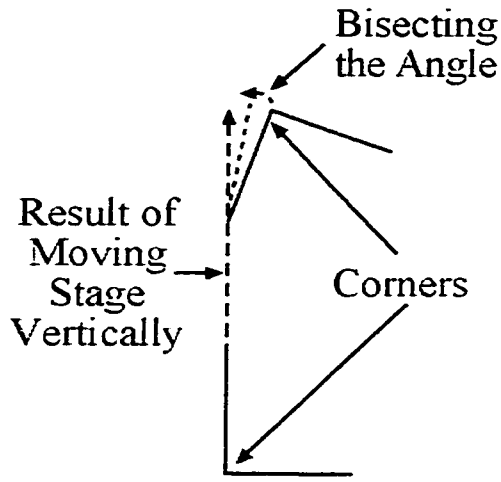

Figure A.9 Procedure for setting the stage rotation.

Subsection A.3.5 Aligning the Sample

The section described how to use alignment markers on the chip to align consecutive lithography steps.

59. Zoom out to magnification 200×, switch to "BUP" mode, and position the top right corner in the cross-hairs.
60. When designing a device pattern, the position of the top right corner is specified in microns as (X_c, Y_c). The cross-hairs are centered at the origin; so the corner must be moved to (X_c, Y_c). The stage control uses units of mm, so, it is used to move ($X_c/1000 + 0.4$, $Y_c/1000$) as described in Step 23. The extra 0.4 mm in the X-axis corrects for an image shift that occurs when switching to computer control of the SEM beam.
61. Switch to "PIC" mode, and press "1" to go to screen 1.
62. Turn the "BEAM BLANKING" switch to the "EXT" (external) position.
63. There is a Pomona box next to the beam current measurement switch. Flip the Pomona box switch towards you.
64. Press the "SLOW" button to switch to slow scan mode, and turn down the brightness using the "BRIGHTNESS" knob until the left screen is dark.
65. Enter the command "al align_file" where "align_file.dc6" is the full name of the alignment file.
66. Press "SPACE" to proceed to the first alignment screen (Fig. A.10(a)). Press "J" twice to set the color scale so white represents maximal signal and black minimal signal. Press "P" to toggle between the two screen magnifications. Press "B" to toggle the scan on and off.
67. With "NUM LOCK" enabled, use the "2" and "8" keys to move the color scale up and down. Use the "4" and "6" keys to widen and narrow the color scale. A good

starting point for optimizing the contrast is to set the color scale equal to the data range.

68. Once the corner is visible[31], use the arrow keys to move the marker outline over the image of the corner. The two numbers (X0, Y0) at the bottom right of the screen correspond to the position of the marker outline in microns; so, the stage control is told to move (-X0/1000, -Y0/1000) to move the corner back to center.
69. Press "B" to turn on the beam, then "O" to rescan and overwrite the current image.
70. Repeat Steps 67-68 until the corner is at the origin, *i.e.* (X0, Y0) = (0, 0).
71. Press "ESC" twice to reach the main menu. Change the magnification if necessary.
72. Repeat the alignment procedure outlined in Step 65-71 for the magnification 20× and 200× alignment markers.
73. The contrast is best right after starting the program; so, for the magnification × 1000 (final) alignment markers, quit the alignment program and restart, as if on Step 64.
74. Use the number keys to change the color scale to match the data range, as described in Step 66.
75. Align as in Steps 65-70 until the markers are within 500 nm of their desired position.
76. Rotation in the sample can be electronically corrected. Press the "INS" key to toggle between four modes, as indicated in the top right corner of the screen:
    - **ALL**: Move both windows together
    - **1**: Move window 1 only
    - **2**: Move window 2 only
    - **MAG**: Adjust the electronic magnification of the image
77. Toggle between the "1" and "2" modes, and align each marker separately. The relative positions of the two markers is used by the program to calculate a rotation matrix. When satisfied, press the "SPACE" key to apply the rotation matrix, rescan the image, and move the marker outlines back to the origin.
78. After both windows have been scanned, the "OVERWRITE" message will disappear, and use the "B" key to turn off the scan beam. If a smoother image is desired, allow a few scans to be averaged before turning off the beam.
79. Iterate Steps 76-77 until both alignment markers fall within the marker outlines.
80. Press "ESC" once, then "ENTER" twice to save the alignment matrix (translational and rotational corrections).

[31] Sometimes the stage does not move exactly where it should, and the marker is not visible in the scan window. The best approach is to scan in an outwardly growing spiral.

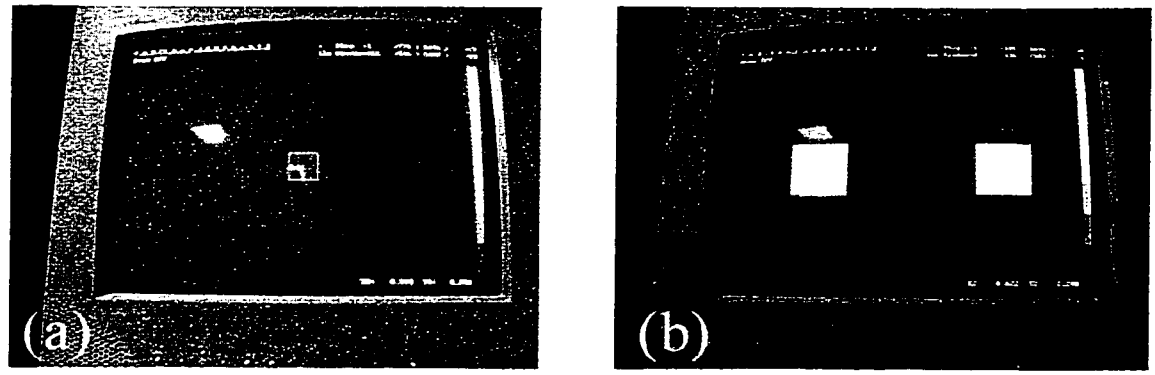

Figure A.10 Screen shots of alignment program when aligning to (a) corner of chip and (b) magnification 1000× alignment markers.

Subsection A.3.6 Writing the Pattern

This subsection describes the procedure for writing the lithography pattern once alignment has been completed.

81. Enter "pg pattern_name a" where "pattern_name.dc6" is the full name of the pattern file. The "a" flag at the end instructs the "pg" program (pattern generation) to use the alignment matrix.
82. Follow the on-screen instructions for setting the magnification and beam current.
83. Press the "SPACE BAR" when prompted by the computer.

Subsection A.3.7 Turning Down the Filament

This subsection describes the procedure for turning down the filament and shutting off the SEM after writing the lithography pattern.

84. Set CL = 16.
85. Use the stage control joystick to move the chip ~ 5 mm to the right, and out of the field of view.
86. Set the magnification to 100×.
87. Turn the Pomona box switch away from you.
88. Turn the "BEAM BLANKING" switch to "OFF".
89. Press the "PIC" button, and turn up the "BRIGHTNESS" knob until an image appears on the left screen.

90. Recheck (Step 56) the current values for the condenser lenses used in writing. If the pattern does not develop properly, this will help determine if it was due to an incorrect beam dosage setting or to a fluctuation in the beam current.
91. Gradually turn the filament knob CCW over a period of ~ 5 s.
92. Press the "ON" button to turn off the accelerating voltage.
93. Press the "MEMO" key, highlight the "ACC15 WD39" setting, and press the "L" key.
94. Turn the "SCAN ROTATION" switch to "OFF", turn the white ammeter switch from "AEM" to "ALARM", turn the magnification dial to maximum (300,000×), press the "SLOW" button, and turn the "BRIGHTNESS" knob CCW until the left screen is dark.
95. Press the "PF1" key to turn off the display on the right screen.

Subsection A.3.8 Unloading the Sample

This subsection describes removing the sample from the SEM after writing the lithography pattern.

96. Turn stage rotation to "000".
97. Set the working distance to "39".
98. Press "EXCH" and then "ENTER" on the stage control to return the stage to the loading position (X, Y) = (25, 35).
99. Reverse the loading steps as described in Subsection A.3.2.
100. Put sample mount holder back in dessicator bell jar.

Section A.4 Evaporating Ni:Au:Ge Ohmic Contacts

Thermally evaporating ohmic contacts consists of three steps: preparing the chips for evaporation, evaporating Ni, Au, and Ge, and lift-off of unwanted metal.

Subsection A.4.1 Chip Preparation

1. Sand the ohmic evaporation stage clean of metal from previous evaporations.
2. Clean the stage with IPA and a TekWipe.
3. Pour 10-20 ml of a solution (1:5 by volume) of ammonium hydroxide (NH_4OH) and water (H_20) into a plastic, disposable beaker.
4. Dip each chip in the solution for 3 s.
5. Immediately blow the chips dry with UHP N_2 until all the NH_4OH is gone.
6. Examine the chips under the optical microscope to see if any particles got on the chip. If there are, put the chips into a plastic, disposable beaker filled with 20-30 ml of IPA and sonicate the beaker in the ultrasound cleaner for 1 s.
7. After sonication, blow the chips dry with UHP N_2.
8. Arrange the chips for evaporation on the stage, keeping them as close to the center of the stage as possible, but separated from each other by ~ 1 cm.
9. Taking a wooden applicator stick with a tapered end, apply carbon paint to each edge of each chip, like mounting for electron-beam lithography.
10. Wait 3 min. for the carbon paint to dry.
11. Check all the chips are secure by placing a gloved hand over the evaporation stage and turning the stage upside down. Gently shake the stage to confirm that no chips fall off.
12. Reaffix any loose chips[32] as in Step 9, and once all chips are secure, proceed to Evaporation.

Subsection A.4.2 Evaporation

13. The metal is evaporated using a thermal evaporator (Fig. A.11), which consists of a power supply connected to metal arms inside a bell jar pumped out to ~ 0.5 μT by a cryopump.
14. Before starting the evaporation, confirm
    - the cryopump is working (T = 15 K)
    - the gate valve (GV) is open
    - pressing the "XTAL TEST" button on the crystal monitor yields a reading between 4000 [new crystal] and 5000 [end of crystal life], and the monitor is off
    - the ion gauge is off

[32] But there really should be none!

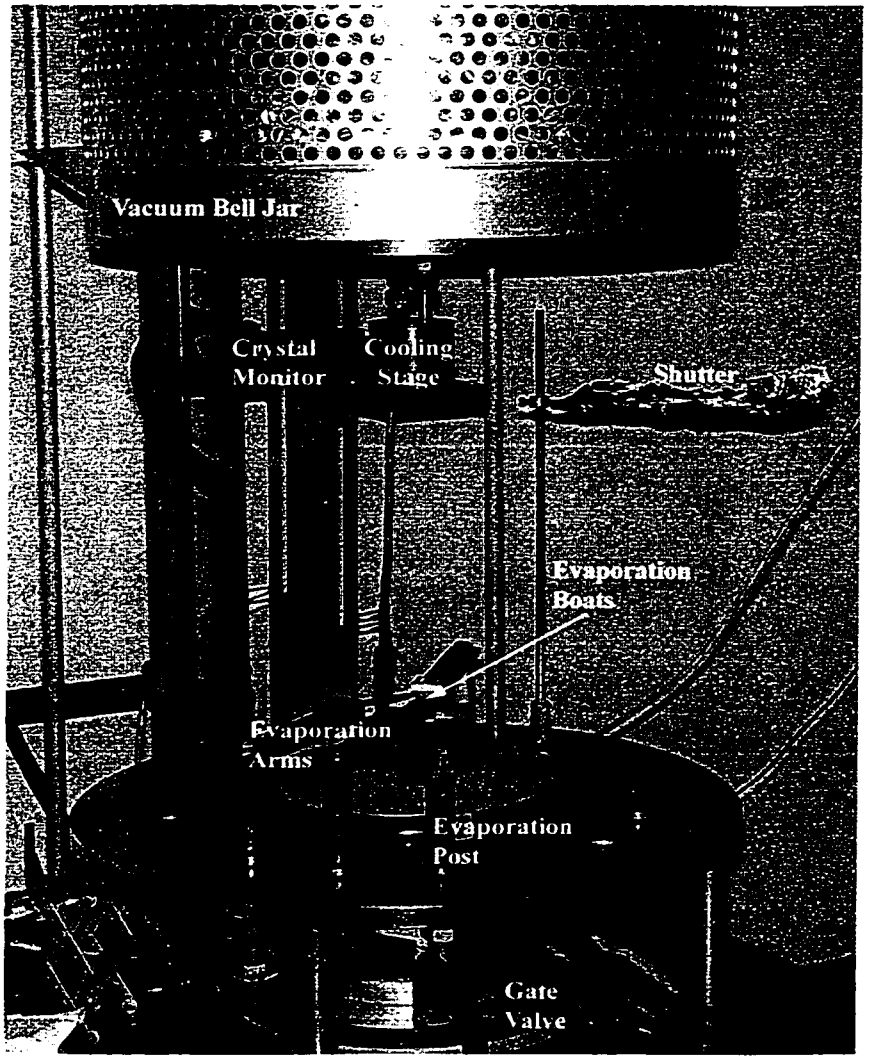

Figure A.11 Ohmic contact evaporator.

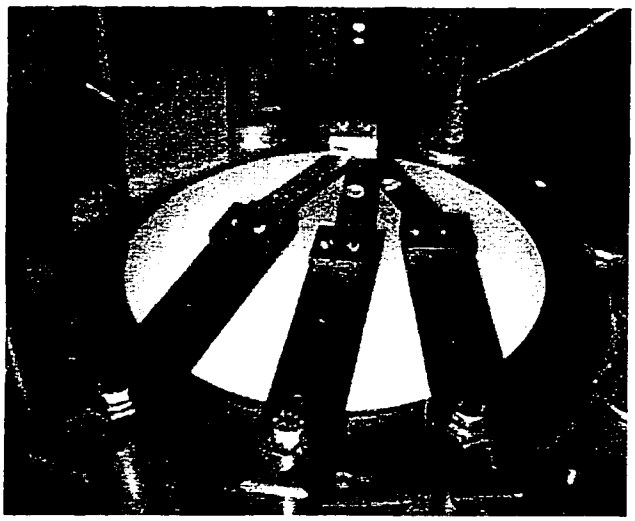

Figure A.12 Ohmic contact evaporation arms and attached evaporation boats (Ni, Ge, and Au from left to right).

15. Close the GV, insuring you hear a click.
16. Open the vent valve (VeV) a quarter-turn. It will take 2 to 3 minutes to vent the chamber to atmosphere.
17. Once vented, close the VeV, and raise the the bell jar until you can see the cooling stage.
18. At a location where both the cooling stage and evaporation arms can be seen, tear a small hole (~ 1/4" diameter) in the Al foil lining the bell jar.
19. Wipe the bell jar O-ring clean of any metal flakes.
20. Check the mount plate is level with the crystal meter.
21. The evaporation arms and metals are kept in the lockbox in the outer cleanroom. All arms are labeled with stamped letters ("NI", "AU", "GE", and "GND"). Place the "NI" arm on Post 1, the "GE" arm on Post 2, the "AU" arm on Post 3, and the "GND" arm on the ground Post, which lies opposite Posts 1-3. Make sure the ends of the arms will not tear the Al foil lining the bell jar.[33]
22. Secure the arms to the posts, and loosed the bolts by 1/4 turn to decouples the arms from the vibrations from the cryopump.
23. Place an evaporation boat between each arm and the ground arm as shown in Fig. A.12, using a thicker boat (RDM – Item # S47-020W) for Post 1, and dimpled boats (RDM – Item #S9A-010W) in Posts 2 and 3. Keep the three boats as close as possible. Once satisfied with their position, clamp them to the arms, and check none of the boats are under stress or strain so they will not crack when heated.
24. Cut four 1/4" lengths of 1 mm diameter 99.9945% nickel wire (AAI – Item #10929), and place them lengthwise in the boat held between Posts 1 and Ground.
25. Place one piece of 99.999% germanium (AAI – Item #10191) in the dimple of the boat held between Posts 2 and Ground.

[33] Another problem that arises if the arms contact the Al foil is the arms will then be electrically shorted to each other.

26. Place about twelve 1 mm^3 pieces of 99.99% gold into the dimple of the boat held between Posts 3 and Ground.
27. Attach the evaporation stage to the cooling stage, and close the shutter to cover evaporation stage and the chips. Check that opening and closing the shutter will not scratch the chips.
28. Lower the bell jar, and hold it down. Then, open the roughing valve (RV).
29. Pump the chamber down to ~ 150 mT (~ 5 minutes).
30. Close the RV, and open the GV. The pressure should drop quickly to < 10 mT.
31. Turn the ion gauge on, and select the log scale.
32. Degas the ion gauge filament for 30 seconds.
33. It is necessary to pre-melt the metals because vibrations from the cryopump can cause the metals to jump out of the boats[34]. Begin with using the post selector to complete the electrical circuit between Posts 3 and Ground.
34. Close the switch to the power supply.
35. Using the potentiometer, turn up the power in 5% increments every 15 seconds until the Au melts.
36. After the metal melts, turn down the potentiometer to 0% at a rate of ~ 50%/minute.
37. Turn off the switch to the power supply.
38. Repeat Steps 33-37 for Posts 2 (Ge) and 1 (Ni).
39. Set the sign hanging on the bell jar so it reads "In Use", leave, and wait ~ 1 hour for the chamber to pump down to ~ 0.5 μT.
40. Open the air cooling valve by a quarter-turn, and evaporate metals in the following sequence similarly to the pre-melt sequence described in Steps 33-37.

Metal	Evaporate with shutter closed[35] (Å)	Evaporate with shutter open[36] (Å)	Typical potentiometer setting (%)	Typical evaporation rate (Å / s)
Ni	50	50	50	1
Au	50	50	45	2
Ge	50	250	55 – 60	1.5
Au	50	450	45 – 50	2 – 2.5
Ni	50	100	50 – 55	1 – 1.5
Au	50	400	45 – 55	2 – 2.5

Table A.2 Sequence of metals evaporated for ohmic contacts.

41. With the crystal monitor off, set the density for the metal being evaporated.
42. Turn on the crystal monitor, and press the "ZERO" button until the meter reads "0".
43. The meter will display in angstroms the thickness of metal evaporated.
44. Use the crystal monitor to determine the thickness of metal evaporated
45. Turn off the crystal monitor after each metal.
46. After completing the evaporations, turn off the ion gauge.

---

[34] Otherwise, one can return to find all the metal is out of the boats, and one has to repeat the venting, loading, and pumping. The lesson was learned when it happened three times in one very long day.
[35] We evaporate 50 Å of metal with the shutter closed to bake off any surface contaminants.
[36] When evaporating a thin layer (< 50 Å), we use a slower rate so the metal wets better to the GaAs. For thicker layers, we evaporate the first 50 Å at a slow speed, and use a faster rate for the remainder.

47. Leaving the cooling air on, wait 15 minutes for everything to cool. This is important not only for the sample, but also for the evaporation arms, which will oxidize much more rapidly if exposed to atmosphere while they are still hot[37].
48. Close the GV, making sure you hear a click.
49. Open the VeV a quarter-turn, and wait 2 to 3 minutes for the chamber to vent to atmosphere.
50. Raise the bell jar until you can see and access the evaporation stage.
51. Loosen the screws holding the evaporator boats and throw away the boats.
52. Loosen the hex nuts holding the evaporator arms and replace them in the lockbox in the outer cleanroom.
53. Remove the evaporation stage from the cooling stage.
54. Wipe away any metal flakes that fall down, and wipe clean the bell jar O-ring.
55. Pump the chamber down as described in Steps 28-30.

Subsection A.4.3 Lift-off

56. After evaporating the metal, acetone is to dissolve the PMMA under the unwanted metal, which then lifts off the chips, leaving metal only where the PMMA was patterned.
57. Using a scalpel, gently cut the the carbon paint between the bottom of each chip and the top of the evaporation stage. As GaAs cleaves very easily, be careful to apply pressure underneath the chip and not to the side edge of the chip. Use only enough pressure to get the chip loose.
58. Place each chip in a 50 ml plastic, disposable beaker, and fill the beaker with ~ 20 ml of acetone. Cover the beaker with Al foil, and form a good seal along the top rim of the beaker so the acetone will not evaporate.
59. After ~ 1 hour, use the squeeze bottle to spray the chip with acetone. The unwanted metal should just wash off.
60. Place the small petri dish cover dedicated for acetone, and spray enough acetone into the petri dish cover to cover the chip. Then, use the optical microscope to check that all the unwanted metal is gone. It is very important not to let the chip dry until lift-off is complete. Otherwise, metal that would have been lifted off will adhere quite firmly onto the chip.
61. If there is still some metal or PMMA clinging to the chip, spray the chip with acetone, put it back in the acetone-filled beaker, and reform the Al foil seal. Let it sit for an additional hour.
62. Repeat Steps 58-60 until all the unwanted metal is gone.
63. If not all the metal lifts off after soaking in acetone overnight, then it may be necessary to sonicate the chip with the ultrasound. As sonication can remove the wanted metal, it is best to sonicate for short intervals (< [redacted] s).
64. Once all the unwanted metal has lifted off, spray the chip with methanol and blow dry with UHP N_2.

[37] Not to mention the fact they are hard to handle when hot!

Section A.5 Annealing

This sections describes annealing ohmic contacts after evaporation so they diffuse into the heterostructure and make electrical contact with the 2DEG.

1. Confirm
   - The thermocouple is working
   - The potentiometer is off
   - The O-ring (3 5/8" diameter × 0.1" tube diameter) is in good condition
   - Annealing chamber is closed, everything is off.
2. Open the chamber, and place the chip on the tungsten strip, as close as possible to thermocouple.
3. Close chamber, tightening the screws until you see the O-ring forms a good seal.
4. Open the valve to the cylinder of compressed exchange gas (80% helium, 20% hydrogen) and adjust the regulator until the bottom of the silver ball in the flowmeter reads "3".
5. Turn potentiometer on to the "140 V" setting.
6. Turn on the thermocouple reader, making sure it is in the "K" mode.
7. Table A.3 lists in order the steps involved in annealing. For each step, slowly turn up the potentiometer until the thermocouple reads the appropriate temperature. The time indicated is the time after the strip reaches the target temperature. As the tungsten strip will continue to heat, monitor the temperature and adjust the potentiometer to maintain the target temperature.
8. After each temperature step, check the flowmeter still reads "3", and adjust the regulator if necessary.

Temperature (°C)	Time (s)	Purpose
110	60	Boil off moisture
250	20	Prime the chip
410 – 415	12 - 15	Anneal the metal

Table A.3 Sequence of temperatures and durations for annealing ohmic contacts.

9. Turn the potentiometer down to 0, and turn up the gas flow to cool the heating strip.
10. After the temperature drops below 45 °C, open the chamber, and remove the chip.
11. Rotate the chip 180°, and repeat the annealing process. After this step, the contact should look like the surface of a cheese pizza. If they are still smooth, then further annealing may be necessary.

Section A.6 Evaporating Cr:Au Gates

Forming Cr:Au gates requires three steps: preparing the chips for evaporation, evaporating the ohmics, and lift-off of unwanted metal. This process is very similar to that for thermally evaporating Ni:Au:Ge ohmic contacts. There is only one difference in chip preparation: the chips must be dipped in 1:5 30% NH_4OH:H_2O for 5 s to remove any oxides on the surface and aid adhesion of the gates. The section discusses the differences in operating the thermal evaporator dedicated for Cr:Au gates.

1. Before starting the evaporation, confirm
   - the cryopump is working (T = 15 K)
   - the gate valve (GV) is open
   - the crystal monitor displays "READY" when turned on
   - the ion gauge is off
2. Close the GV, insuring you hear a click.
3. With the crystal monitor and ion gauge off, open the vent valve (VeV) a quarter-turn. It will take 2-3 minutes to vent the chamber to atmosphere.
4. Turn on the power switches for the mechanical roughing pump and the hoist to raise and lower the bell jar.
5. Once vented, close the VeV, and turn the house switch to the "RAISE" position to raise the bell jar until you can see the cooling stage.
6. Pick a location where you can see both the cooling stage and evaporation arms, and tear a small hole (~ 1/4" diameter) in the Al foil lining the bell jar.
7. Wipe away any metal flakes that fall down, and wipe clean the bell jar O-ring.
8. Check the mount plate is level with the crystal meter.
9. The evaporator has three separate posts and one ground post. Normally, evaporation arms are on Posts 1, 2, and Ground.
10. Carefully bend an evaporation arm into a hill profile, and place it between Posts 2 and Ground.
11. Place a Cr rode between Posts 1 and Ground, using the notch cut into the Ground arm to accommodate the Cr rod.
12. Once satisfied with their positions, clamp the rod and the boat to the arms with the screws, checking the boat is not are under stress or strain. If necessary, use a boat fragment for a shim between the evaporation boat and the Ground Post to create better electrical contact.
13. Place about five 1 mm^3 pieces of gold (Au) from the lockbox in the outer cleanroom into the dimple of the boat held between Posts 2 and Ground.
14. Place a Cr rode between Posts 1 and Ground, using the notch cut into the Ground arm to accommodate the Cr rod.

15. Attach the evaporation stage to the cooling stage, and close the shutter so the evaporation stage and the chips are completely covered and cannot see the evaporation boats. Take care that opening and closing the shutter does not scratch the chips.
16. Turn the hoist switch it "LOWER".
17. As the bell jar lowers, push on it so it lowers in the correct poistion.
18. Once the bell jar down, open the roughing valve (RV).
19. The hoist power switch will turn off once the pressure drops below the safety interlock value. At that point, turn the hoist switch to the middle position and the hoist power switch off.
20. Pump the chamber down to ~ 150 mT (~ 5 minutes).
21. Close the RV, and open the GV. The pressure should drop quickly (relative to when roughing with the mechanical pump) to < 10 mT. Then turn off the mechanical pump power switch.
22. Turn on the ion gauge.
23. Turn on the switch to the power supply.
24. Use the post selector to complete the electrical circuit between Posts 1 and Ground.
25. Using the potentiometer, dial up the power to 10%. The pressure will quickly rise due to moisture boiling out of the Cr rod. Once the pressure drops back down to ~ 50 μT, turn the power down to 0%.
26. Switch off the power supply.
27. Use the post selector to complete the electrical circuit between Posts 2 and Ground.
28. Then, switch on the power supply.
29. Using the potentiometer, dial up the power in 5% increments every 15 seconds until the Au melts.
30. After the metal melts, turn down the potentiometer to 0 at a rate of ~ 50%/minute.
31. Degas the ion gauge filament for 30 seconds.
32. Switch off the power supply.
33. Set the sign hanging on the bell jar so it reads "In Use", leave, and wait ~ 1 hour for the chamber to pump down to ~ 0.5 μT.
34. Open the air cooling valve by a quarter-turn, and evaporate metals in the following sequence:

Metal	Evaporate with Shutter closed[38] (Å)	Evaporate with Shutter open[39] (Å)	Typical potentiometer setting (%)	Typical evaporation rate (Å / s)
Cr	50	50	25-30	1
Au	50	400	40-45	1-2

Table A.4 Sequence of metals to be evaporated for Cr:Au gates.

[38] We evaporate 50 Å of metal with the shutter closed to bake off any contaminants that have gathered on the surface.

[39] When evaporating a thin layer (< 50 Å), we use a slower rate so the metal wets better to the GaAs. For thicker layers, this becomes overly time-consuming; so, we evaporate the first 50 Å at the same setting as for a thin layer, and use a faster rate for the remainder.

35. Turn on the crystal monitor.
36. Press the "PG" button, and use the "E" button to scroll down the parameter list
37. Enter the density, Z-ratio, and tooling factor,
38. Press the "START" button twice.
39. The meter will display in angstroms the thickness of metal evaporated.
40. Press the "STOP" button when done with a particular metal.
41. After completing the evaporations, turn off the crystal monitor and the ion gauge.
42. Leaving the cooling air on, wait 5 minutes for everything to cool. This is important not only for the sample, but also for the evaporation arms, which will oxidize much more rapidly if exposed to atmosphere while they are still hot[40].
43. Close the GV, making sure you hear a click.
44. Open the VeV a quarter-turn, and wait 2-3 minutes for the chamber to vent to atmosphere.
45. Raise the bell jar as described in Steps 4-5.
46. Loosen the screws holding the evaporator boats and throw away the boats.
47. Remove the evaporation stage from the cooling stage.
48. Wipe away any metal flakes that fall down, and wipe clean the bell jar O-ring.
49. Lower the bell jar and pump out the chamber as described in Steps 15-20.
50. Turn off the power switch for the mechanical pump and the hoist.

[40] Not to mention the fact they are hard to handle when hot!

Section A.7 Ion Miller

The ion miller is a directed ion beam system used for dry etching. The ion milling process consists of three steps: preparing and mounting the chips, exposing the chips to a directed ion beam, and removal of the PMMA.

Section A.7.1 Chip preparation

1. Chips to be etched should be mounted 2 1/2" below and 5/8" to the right of the top left corner of the loader plate. This is the center of the ion beam.
2. Mount the chips with carbon paint, as for electron-beam lithography.
3. Wait 3 min. for the carbon paint to dry.
4. Test that all the chips are on securely by placing a gloved hand over the evaporation stage and turning the stage upside down. Gently shake the stage to confirm that no chips fall off.
5. Reaffix any loose chips[41] as in Step 2, and once all chips are secure, proceed.

Section A.7.2 Ion Milling

The ion miller uses a gun with a tungsten filament which emits electrons that ionize the etching gas, argon. The argon ions are accelerated toward a target stage in the chamber, which is evacuated to ~1 μT. Details of its construction (Anand 1995, Spalding 1990) and operational principles (Kaufman 1984) can be found elsewhere.

6. Before entering the cleanroom, go to the back alley, turn on the mechanical roughing pump, and open the valve to the ion miller.
7. Remove all the bolts from the door of the ion miller before venting; otherwise, an overpressure can build up as the chamber is vented.
8. Open the bellows valve closest to the chamber.
9. Open the vent valve leading to the nitrogen gas line.
10. Open the valve (on the wall) to the nitrogen gas system a quarter turn.
11. The chamber should vent in ~ 5 minutes, at which point, the door will open ~ 2" wide. Once the chamber is vented, close the valve to the nitrogen gas system, then the vent valve.
12. Open the door fully, taking care not to catch the electrical cable to the gun.

[41] There shouldn't be any this time either!

13. Align the markings labeled "3" and "90 DEG" on the top of the support column. Face 3 of the target stage is now facing the ion gun. Attach the loading plate to Face 3 using a screw for each corner. The loading plate should lie both for good thermal coupling to the water-cooled target stage and so the ion beam is at normal incidence.
14. Turn the target stage 180 degrees.
15. Close the chamber door, making sure the O-ring is well-seated.
16. Insert and tighten a bolt into every other tapped hole.
17. Open the bellows valve further away from the chamber. As the roughing pump has been turned on and the outside valve opened (Step 6), this opens the chamber to the mechanical pump. Evacuate the chamber to ~ 150 mT, which should take ~ 2 min.
18. While roughing out the chamber, open the toggle valve between the mass flow controller (MFC) and the gun to pump out gas in the lines.
19. Once the chamber pressure reaches 150 mT, close both bellows valves, starting with the one closer to the chamber.
20. Open the gate valve to the cryopump. The pressure should drop rapidly. If it does not, make sure the cryopump temperature is ~ 15 K. If the temperature is higher than that, then the cryopump needs to be regenerated.

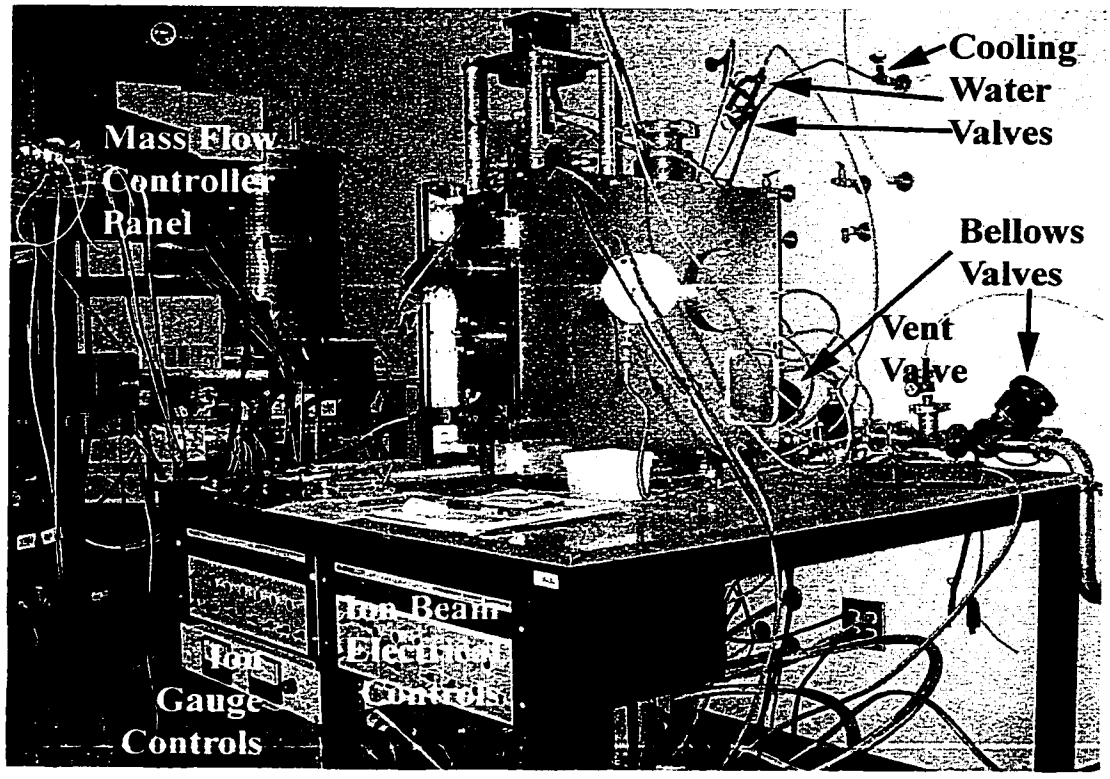

Figure A.13 Ion miller system.

21. Set the ion gauge to the 10^{-4} T scale and turn it on. Within 20 s, the pressure should drop below 0.1 mT. If it stays around 0.2 mT, then most likely, the rubber gasket on the other target stage has not made a good seal. This is quickly remedied by spritzing a small amount of acetone around the support column of the other stage. The acetone will be absorbed by the gasket and cause the gasket to expand, making the seal good.
22. Open the cooling water valves, starting the with low pressure (outlet) valve.
23. Degas the ion gauge filament for 1 min.
24. Check the MFC is powered but off. If its power supply is off, turn on the power supply so the MFC can warm up and settle.
25. Pump on the chamber until the pressure is at or below 2 μT. This takes ~ 1 hr.
26. Open the main valve to the argon gas cylinder and the toggle valves between the cylinder and the MFC. The toggle valve to the chamber has previously been opened (Step 17); so, the mass flow controller now completely controls the gas flow to the chamber.
27. Set the ion gauge to the 10^{-4} T scale, and set the MFC to AUTO Mode and increase the flow (to ~ 8 to 9 sccm) until a chamber pressure of 0.18 mT is reached.

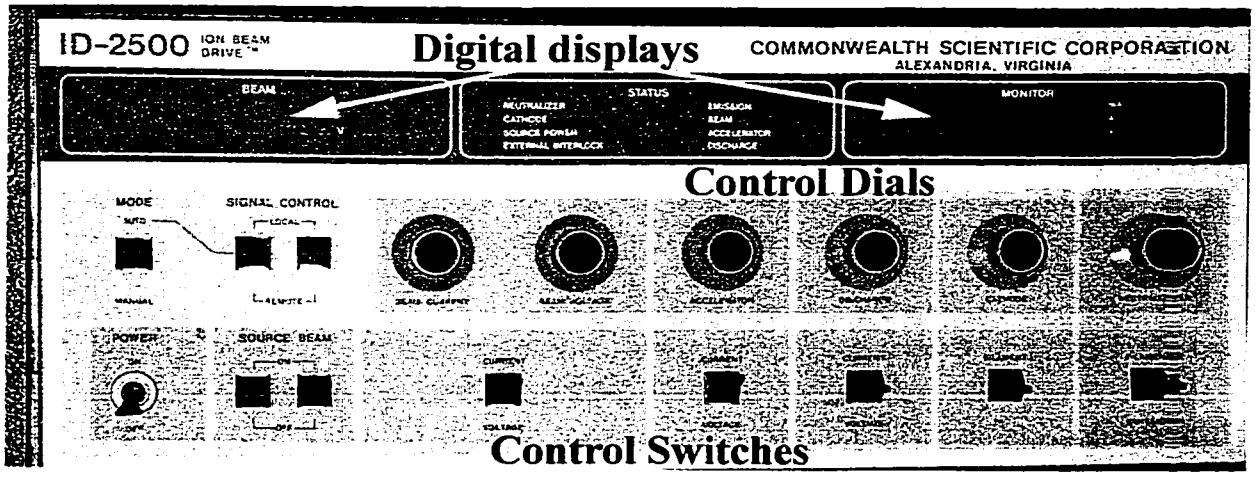

Figure A.14 Electrical control panel for ion miller system.

28. Make sure all the dials on the electrical control panel of the ion miller power supply (Fig. A.14) are turned off (CCW), and then turn on the main power switch. The External Interlock indicator light should turn on.
29. Wait 3 min. for the power supply to warm up and for the chamber pressure to settle. The desired operating pressure for the chamber is 0.2 mT, if necessary, adjust the MFC flow rate.
30. Turn on the source switch. The "NEUTRALIZER", "CATHODE", and "SOURCE POWER" indicator lights should all turn on. In addition, the "DISCHARGE" indicator light should turn on and blink.

31. While holding the "NEUTRALIZER" switch up, towards the "FILAMENT" setting, turn the "NEUTRALIZER" dial clockwise until a current of 7.25 A is read on the right-hand digital display.[42]
32. Hold the "DISCHARGE" switch down, towards the "VOLTAGE" setting, and turn the "DISCHARGE" dial clockwise until a voltage of 40 V is read on the right-hand digital display.[43]
33. Hold the "CATHODE" switch up, towards the "FILAMENT" setting, and turn the "CATHODE" dial clockwise until the "DISCHARGE" indicator light stops blinking, and remains on, indicating discharge of electrons by the main gun filament. This should happen at a current ~ 5 to 6 A.
34. Turn on the beam switch. The "EMISSION", "BEAM", and "ACCELERATOR" indicator lights should all go on.
35. Hold the "BEAM" switch down, towards the "VOLTAGE" setting, and turn the "BEAM VOLTAGE" dial clockwise until a voltage of 500 V is read on the left-hand digital display.[44]
36. Hold the "ACCELERATOR" switch down, towards the "VOLTAGE" setting, and turn the "ACCELERATOR" dial clockwise until the right-hand digital display reads 100 V.[45] The beam current will rapidly decrease and then saturate.
37. Hold the "DISCHARGE" switch down, towards the "VOLTAGE" setting, and if necessary, use the "DISCHARGE" dial to adjust the discharge voltage back to 40 V.
38. Hold the "CATHODE" switch up, towards the "FILAMENT" setting, and turn the "CATHODE" dial clockwise until the beam current is 23 mA, as read on the left-hand digital display.
39. Check that all parameters are close to their nominal values:

---

[42] The Neutralizer filament sits in front of the accelerator grid and emits electrons to neutralize the positive argon ions bombarding the target. This prevents insulating targets from building up charge and deflecting the ion beam. We use ~ 7 A of current through a similar gauge filament to generate the electrons which ionize the argon atoms, so 7.25 A should generate a sufficient number of electrons.

[43] The Discharge voltage establishes the energy of the electrons emitted from the gun filament. As it takes 42 eV to doubly-ionize argon, 40 V maximizes the chances of creating Ar^{+} without creating Ar^{++}, which will have twice the desired energy after acceleration.

[44] The Beam voltage establishes the energy of the ions.

[45] The Accelerator voltage creates a barrier to prevent electrons from backstreaming into the gun, and yielding a false beam current reading.

Parameter	Nominal Value	Press Up/Down on Switch to Read Value	Displayed on Left/Right Digital Display
Beam Voltage	500 V	Down	Left
Accelerator Voltage	100 V	Down	Right
Discharge Voltage	40 V	Down	Right
Beam Current	23 mA	N/A[46]	Left
Accelerator Current	1.0 – 1.2 mA	N/A	Right
Discharge Current	0.65 – 0.75 A	Up	Right
Cathode Current	6.8 – 7.1 A	Up	Right

Table A.5 Ion miller parameter settings.

40. Quickly rotate the target stage so Face 3 is towards the gun, aligning it as described in Step 12.
41. After the desired etch time, quickly push down on the "BEAM", then "SOURCE" switches to stop the beam.
42. Turn all the dials on the electrical control panel counter-clockwise until they are fully off, and then turn of the main power switch.
43. Turn off the ion gauge filament.
44. Close the gate valve.
45. Turn the MFC flow rate to maximum. This floods the chamber with argon, allowing the filament to cool in a neutral gas, *i.e.* low oxygen, environment.
46. For each minute of etching, allow five minutes of cooling.
47. Turn the MFC flow rate to zero, and turn the MFC off.
48. Close the main valve to the argon gas cylinder and the three toggle valves from Steps 17 and 25.
49. Vent the chamber as described in Steps 7-10.
50. Remove the loading plate.
51. Evacuate the chamber as described in Steps 14-19. However, only leave the gate valve open for a few seconds.
52. Close the gate valve.
53. Close the cooling water valves, beginning with the two high-pressure valves.

Subsection A.7.3 PMMA Removal

Removing PMMA is exactly like the lift-off technique for in metal deposition. If soaking and sonicating in acetone does not remove all of the PMMA, especially at the edges of etch trenches, the oxygen reactive ion etch (RIE) system can be used to clean off

[46] The beam and accelerator currents are displayed by default.

the remaining PMMA. Typically, 30 to 60 seconds in the oxygen RIE at 75 W of power is sufficient. If the PMMA still remains, one can etch for more time, but after a cumulative 5 min. of etching, it is highly unlikely the PMMA will be removed. At that point, it is better to either accept the PMMA or discard the chip.

Section A.8 Oxygen Reactive Ion Etch (descummer)

This section describes using an oxygen reactive ion etch (O_2 RIE), or descumming, to clean chips. It is most useful for removing PMMA that was not dissolved by acetone.

1. Turn on the power switches for the mechanical pump and the descummer.
2. Open the main valve to the O_2 cylinder and the valve leading to the descummer.
3. Open the door to the chamber. Release the spring clip holding the cover in place, and remove the cover.
4. If the rubber gasket looks dry, apply a thin layer of vacuum grease to it.
5. Place the chips to be cleaned in the center of the chamber.
6. Replace the cover and the spring clip.
7. Close the door to the chamber.
8. With the "POWER" switch set to "FORWARD", hold down the "PRESET" switch and use the "CONTROL" knob to set the desired power. 80 W is a good setting for cleaning.
9. Set the etching time (typically 30 s).
10. Press the "START" switch down and release it. After ~ 5 s, the descummer will beep and automatically start pumping out the chamber.
11. When the pressure reaches ~ 250 mT, turn the mass flow controller (MFC) on.
12. The descummer will automatically open the valve between the MFC and the chamber when the pressure has stabilized. This will be marked by a jump in the pressure from $\leq$ 250 mT to ~ 400 to 600 mT.
13. The pressure will drift down to a steady-state value. Adjust the MFC setting so the steady-state value is ~ 500 mT.
14. One the pressure stabilized, the descummer will ignite the oxygen into a plasma, causing the pressure to jump to 600 to 700 mT. Again, the pressure will drift down. Adjust the MFC so the pressure is ~ 500 mT.
15. With the "POWER" switch set to "REFLECTED", use the "RF TUNE" knob to minimize the reflected power, which can usually be tuned to 2 W or less.
16. Now turn the "POWER" switch set to "FORWARD". The value should be within 5% of the preset value.
17. Immediately after the timer goes to 0, turn off the MFC.
18. The descummer will automatically vent the chamber. Once the pressure gauge reads "----", open the chamber door and release the spring clip holding on the cover.
19. Remove the cover and examine the chips. If they are not clean, repeat the process until they are. *N.b.* if the chips are not clean after a total of 5 min. of cleaning, then they are not likely to ever be cleaned.
20. If the chips are clean, replace the cover, and close the chamber door.
21. Close the valves on the O_2 cylinder and turn off the power switches for the mechanical pump and the decsummer.

Section A.9 Hydrofluoric acid (HF) Etching

This section describes using hydrofluoric acid (HF) to etch the AlAs layer of the heterostructure, undercutting the layers containing the quantum well and the two-dimensional electron gas (2DEG) and freeing a cantilever. HF will selectively etch AlAs versus GaAs by a factor of 1,000,000; so, the two GaAs cap layers which encapsulate the quantum well protect the 2DEG. Before performing the HF etch, the chip should be not just free of PMMA but also as clean as possible. For safety, HF etching should be performed with a supervising "buddy" who wears the same safety clothing.

Note on safety : Hydrofluoric acid etching is much more dangerous than any of the other fabrication steps. The acid is odorless, colorless, tasteless, and does not even burn when passing through your skin. Once inside the bloodstream, it catalyzes a reaction that turns your bones into jelly and continues to do so until you die. Given the extreme toxicity, both you and your "buddy" must be vigilant during the entire process as exposure must be *immediately* treated to maximize chances of survival. In the event of exposure, strip and flush the affected areas with water while rubbing calcium gluconate antidote gel over them. Your "buddy" should strip and shower you if you panic. Modesty is of infinitesimal importance as compared to living. You may be naked, wet, and covered in gel, but at least you'll live.

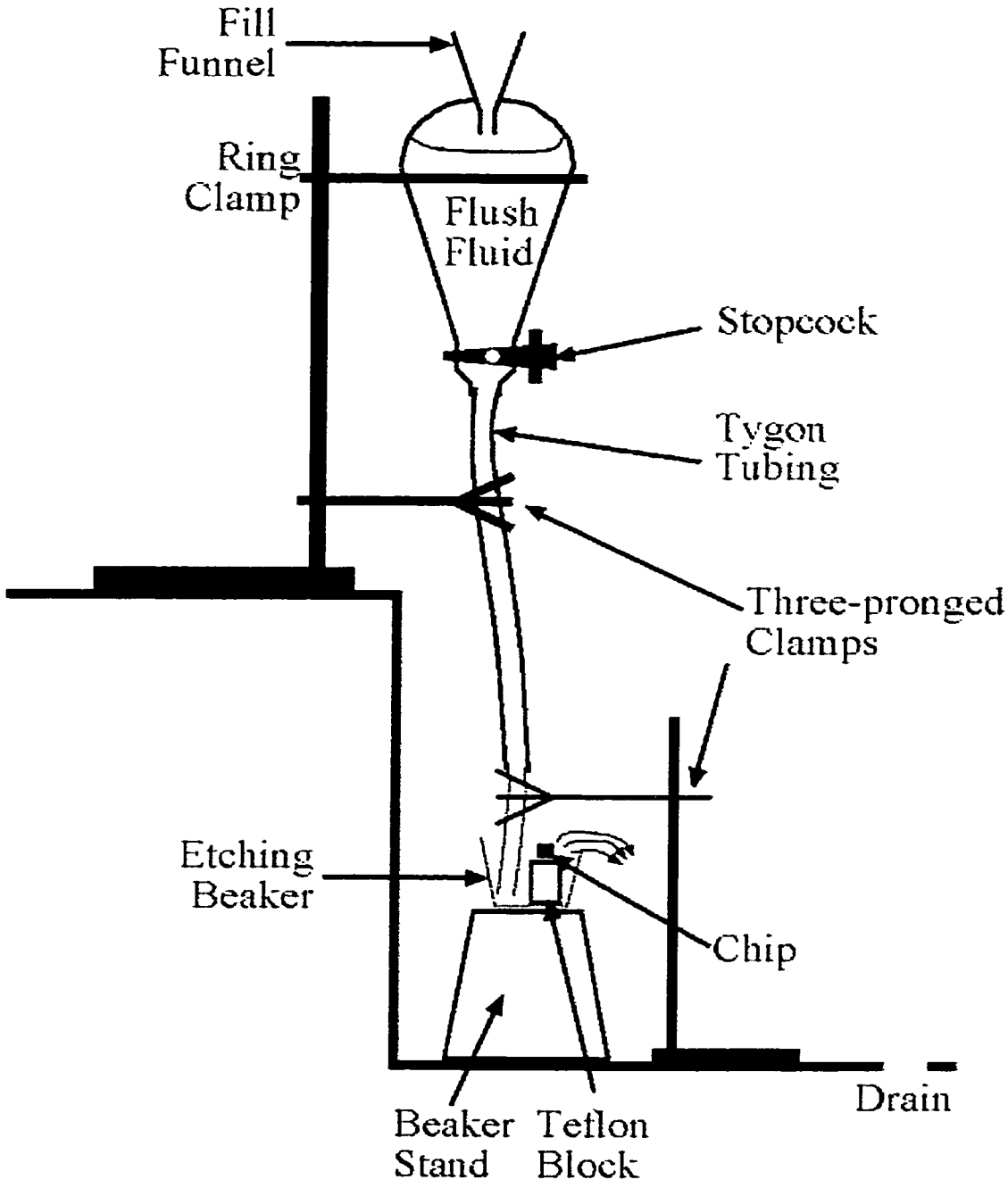

Figure A.15 Setup for HF etching. Held by a ring clamp, a tapered beaker holds the flushing fluid (either water or ethanol), which is carried to the etching beaker through the Tygon tubing. The tubing is held vertical and in place with two sets of clamps. The etching beaker is placed on top of a plastic beaker, which serves as a stand to bring raise the etching beaker for easier access.

1. Set up the etching apparatus as shown in Fig. A.15.
2. Make sure the following are on hand:
   - 49% HF in solution
   - Calcium gluconate antidote gel
   - 1:5 30% NH_4OH:H_2O by volume solution
   - 1:5 38% HCl : H_2O by volume solution
   - 2 liters of distilled water
   - 2 liters of 200 proof ethanol
   - $HS(CH_2)_2(CF_2)_{10}CF_3$ self-assembled monolayer (SAM), dried
3. With the stopper closed, fill the tapered beaker with 1 liter of distilled water. Open the stopcock and allow water to flow until there are no air bubbles inside the Tygon tubing. Then, close the stopcock and refill the beaker.
4. Spray the etching beaker and the Teflon blocks with distilled water. Place the Teflon blocks inside the etching beaker, and place the etching beaker on the beaker stand inside the sink.
5. Place the end of the Tygon tubing inside the etching beaker so it rests in between the Teflon blocks. The end of the tubing should be below the tops of the blocks.
6. Turn on the faucet and point the attached hose towards the beaker stand.
7. Fill three 50 mL plastic beakers with 10 mL of diluted NH_4OH solution, diluted HCl solution, and distilled water, respectively.
8. The diluted HF solution etches $AlGa_{0.2}As_{0.9}$ at a rate of 0.2 μm/sec. As the $AlGa_{0.1}As_{0.9}$ is exposed on all sides, only half the shortest dimension needs to be etched. Set a digital timer for 105% (5% safety factor) of the time needed to go half the shortest dimension.
9. Don the protective apparatus:
   - 1 pair of anti-static gloves (VWR – Item #32915-772)
   - 1 pair of HF-resistant gloves (LSY - Item #8B-37022)
   - 1 HF-resistant frock (LSY - Item #8B-23433)
   - 1 face shield
10. Add 15 mL of distilled water to the etching beaker.
11. Place the calcium gluconate antidote gel in an easily accessible area and unscrew the cap.
12. Keeping the spout pointed away, remove the HF beaker from storage under the sink.
13. Taking care not to squeeze the bottle, unscrew the stopper.
14. Use the plastic graduated cylinder reserved for HF use to measure 2 mL of HF. If too much HF is poured into the cylinder, pour the HF into the sink, and re-measure.
15. Re-stopper the HF storage bottle.
16. Pour the HF from the graduated cylinder into the etching beaker and rinse the graduated cylinder three times with distilled water. Put it aside to dry.
17. Return the HF storage bottle to the storage area under the sink.
18. Using a pair of Teflon tweezers reserved for HF use, dip the chip for 10 s in diluted NH_4OH solution, then 10 s in diluted HCl solution, and then 10 s in distilled water.
19. Place the chip onto the level Telfon block in the etching beaker. Have your "buddy" start the timer as soon as the chip enters the etching solution.
20. Rinse the tweezers with distilled water and set them aside to dry.

21. Immediately after the timer indicates the etching time has passed, open the stopock all the way.
22. Flush the HF with water until an inch of water remains in the tapered beaker. Close the stopcock, and refill the beaker with 1 liter of distilled water.
23. Again, let the water flow until only an inch of water remains in the tapered beaker. Close the stopcock to shut off the flow, but this time fill the beaker with 1 liter of 200 proof ethanol.
24. Wait for the bubbles from the mixing of the ethanol and the water to dissipate, then open the stopcock halfway for a slower flushing of the water.
25. Close the stopcock when an inch of ethanol remains in the tapered beaker. Refill the beaker with 1 liter of 200 proof ethanol.
26. Open the stopcock fully and let all the ethanol flow.
27. Carefully remove the Tygon tubing from the etching beaker, and place it out of the way.
28. Use the hose attached to the faucet to clean the bottom of the etching beaker. Take care no water is sprayed into the etching beaker.
29. Swing the three-pronged clamp out of the way, and use a pair of Teflon tweezers that have not come into contact with HF to lift the entire etching beaker out of the sink. Place the etching beaker onto the counter and make sure the chip remains in solution does not slip off the Teflon block.
30. Remove the other Teflon block, place the chip on the bottom of the beaker, and remove the Teflon block the chip was sitting on.
31. Mix ~ 20 mL of 5 millimolar SAM solution[47] in a new, 50 mL plastic beaker.
32. Use the Teflon carrier to move the chip from the etching beaker to the beaker holding the SAM solution. The chip should never come above the surface of the solution.
33. Seal the top of the SAM solution beaker with Al foil, and cover it with an amber glass bottle. The amber glass will prevent ultraviolet radiation from breaking down the SAM. Leave the chip in the SAM solution for at least 48 hrs. before critical point drying.

[47] The exact concentration is not overly important as long as it is sufficiently strong. Typically, 5 sub-mm diameter clumps of dried SAM in 15 mL of ethanol will form a solution of correct concentration. Mix the solution by shaking the SAM and ethanol together inside a bottle. Use the sonicator to aid in mixing if necessary.

Section A.10 Critical Point Dryer

The critical point dryer (CPD) is used for bringing a free-standing cantilever out of solution. It exchanges ethanol with liquid carbon dioxide (CO_2), and manipulates the pressure and temperature to pass around the critical point of CO_2. Moving around the critical point allows passing from liquid to gas without a phase transition. The gas can then be vented, leaving the sample dry.

1. If it has been used more than 10 times, replace the liquid CO_2 cylinder (MTI – Item #14HS27).
2. If the cylinder has been replaced, also replace the filter element (TRC – Item #8781/82A).
3. Turn on the power to the CPD, and let it warm up for 5 min. Make sure the heating element is off.
4. Check that all valves are closed.
5. Open the main valve of the liquid CO_2 cylinder. The stainless steel tubing leading to the CPD should move in response to the pressure.
6. Remove the cover from the chamber, and clean it with a TexWipe and ethanol.
7. Place the meshed sample holder in the chamber.
8. Fill the chamber half full with 200 proof ethanol.
9. Using the Teflon chip carrier, transfer the chip from the SAM solution into the chamber.
10. Place the chip into one of the chambers of the sample holder, and remove the Teflon chip carrier. Remember, at no point should the chip come out of liquid.
11. Use a plastic pipette to remove ethanol from the chamber until the surface is ~ 1/8" above the top of the sample holder.
12. Seal the chamber, using a pair of pliers to firmly tighten the three knurled nuts.[48]
13. Open the cooling valve (CV) ~ 1/5 of a turn (2 markings).
14. Carbon dioxide will stream around the chamber and cool it. When the temperature gauge reads 0 °C, close the CV. The temperature should settle at –10 °C.
15. Open the inlet valve (IV) by 1.5 markings. The chamber pressure should slowly climb to 400 psi. At that point, the sides of the chamber will begin to "sweat" with condensing CO_2.
16. Let the chamber slowly and completely fill with liquid CO_2. As it gets close to being full, the liquid-air boundary will cross the observation window. Also, the pressure will rise to ~ 800 psi when it is completely full.
17. Close the IV and let the CO_2 and ethanol mix for 5 min.

[48] The O-ring is Teflon covered so it does not interact with and contaminate the CO_2. As such, it does not compress as well, and thus, needs more pressure to make a good seal.

18. Open the vent valve (VV) by 1/10 turn (1 marking) and vent until the chamber is half empty. Ethanol should flow out of the VV outlet line.
19. Close the VV.
20. Open the CV and cool the chamber until the temperature gauge reads 0 °C. Then close the CV.
21. Repeat Steps 15-20 until no more ethanol flows out of the VV outlet line. One test is to hold a piece of white paper underneath the VV outlet line. If there is still ethanol coming out the chamber, it will make clear spots on the paper.
22. Repeat Steps 15-20 one final time.
23. Close the main valve on the liquid CO_2 cylinder. Open the CV by 3 markings to release the remaining CO_2 left in the inlet lines. Once all the CO_2 is gone (the hissing stops), close the CV.
24. Turn on the heating element. The chamber will heat up to ~ 34 °C, and shut off automatically.
25. The heating element should keep the chamber temperature above 31 °C, the critical point temperature. However, the temperature sensor does not seem to be fool-proof, and to insure the chamber temperature remains above the critical point temperature, use a heat gun to warm the chamber until the temperature gauge reaches 36 to 38 °C. The best way to heat the chamber is alternating periods (10 s) of heating and letting the chamber equilibrate. The temperature should continue to rise to ~ 40 °C.
26. As the chamber heats up, the pressure will rise to 1600 to 2000 psi. Above ~ 1700 psi, the overpressure relief valve will open, releasing CO_2 until the pressure reaches ~ 1500 psi.
27. Wait until the overpressure relief valve stops hissing.
28. Attach the flowmeter to the VV outlet line.
29. Turn the bleed valve (BV) until flowmeter reads 5 (silver ball centered on 5 line).
30. As the pressure falls, the flow rate will decline. Open the BV as necessary to maintain a flowmeter reading of 5.
31. Continue to monitor the temperature. If it falls to 34 °C, and the heating element does not automatically turn back on, use the heat gun to warm the chamber, as described in Step 25.
32. If at any point, the chamber begins to cloud over, close the BV immediately. The CO_2 is about to spontaneously condense. Quickly use the heat gun to reheat the chamber, as described in Step 25.
33. Once the pressure falls to 250 psi, there is little chance of spontaneous condensation, and it is fine to open the VV to release the remaining pressure.
34. Once the pressure has dropped to 0 psi, carefully and gently loosen the knurled nuts. Be aware of residual pressure that is not measurable with the gauge.
35. Remove the cover and take out the sample holder and chip. Close the BV and the VV. Replace the cover and nuts.

Section A.11 Wirebonder

The wirebonder is used to attach leads to make electrical contact to the chip. The chip is mounted on a sample holder which can ground all connectors leading to the chip.

1. Turn on the wirebonder, set the stage temperature to 80 °C, and allow it to warm up for 5 min.
2. Thread Au wire through a 45° head[49]. The spool should be placed so the wire runs CCW when looking down the axis of the spool and go through the front hole in the wirebonder arm before going to the wirebonder head.
3. The wire should also go over the guide bar behind the clamp, and through the clamp before going to the head. Use the clamp lever to move the clamp away from the head and the "CLAMP" switch to open the clamp to allow the wire to pass through.
4. Hold the wire so ~ 1/8" protrudes past the tweezers' tips, and bring it toward the back of the wirebonder head, letting the head guide the wire into the hole. Once it is threaded through the head, close the clamp with the "CLAMP" switch, and release the wire.
5. Use the tweezers to take up the slack in the wire.
6. Wearing a grounding strap and anti-static gloves, clamp the sample holder to the stage so the chip is as level as possible. Make sure the chip has sufficient clearance (2 to 3 cm) underneath the wirebonder head. Adjust the stage height if necessary.
7. Use the alligator clip to the sample holder's grounding wire.
8. Position the stage underneath the wirebonder head so the all desired areas are within the range of the motion-reducer mouse control.
9. Set the (Height, Force, Time, Power) settings for both bonds to (10, 3, 3, 2). Set the Loop Height to 10.
10. Press and hold the top button on the mouse control. This will drop the head to the search height. Adjust the Height setting for the first bond until the head is just above where you want to form the first bond.
11. Release the button to make the first bond.
12. Set the Loop Height so the wirebonding head is a few millimeters above the first bond.
13. Adjust the Height setting for the second bond to be equal to the Loop Height.
14. Use the motion reducing mouse control to position the wirebonder head over the desired bonding pad on the chip, and make another bond as in Steps 10-11.
15. Repeat for all the other desired bonds.
16. The wire may occasionally break. If it does, re-thread as described in Steps 3-5.
17. When finished, move the stage out from underneath the head.
18. Unclip the alligator clip from the sample holder's grounding wire.
19. Unclamp the sample holder from the stage.
20. Remove the Au wire spool and replace it in the lockbox in the outer cleanroom.
21. Turn off the wirebonder.

[49] The angle denotes the angle the wire goes through the head.

Appendix B Data Analysis Programs

This chapter describes the IGOR (WMI – Item #10-625) computer programs used to analyze the data presented in this thesis. Any text on a line that follows "//" is a comment and not used in the program.

Section B.1 Small-Signal Drain-to-Source Resistance

The macro "ProcessTable" was used to create a plot of small-signal drain-to-source resistance r_{ds} as a function of gate voltage from a table of data of the drain characteristics of an FET. The table is formatted so the first column contains the values of the drain-to-source voltage V_{DS}, and the following columns are the values of the drain current I_D. The gate-to-source voltage V_{GS} differs by the same amount between consecutive columns of I_D values. Two inputs are required: "TableName", the name of the table of drain characteristics data, and "StepSize", the change in V_{GS} between columns.

```
#pragma rtGlobals=1          // Use modern global access method.

Macro ProcessTable(TableName, StepSize)
        String TableName
                Prompt TableName, "Enter Table Name"
        Variable StepSize
        Prompt StepSize, "Enter size of gate voltage steps between columns, including
sign"
        FitTable(TableName, StepSize)
        Display rdsVals vs GateVals
        Label left "r\\Bds\\M (k-Ohms)"
        Label Bottom "V\\Bgs\\M (V)"
End

Function FitTable(TheTable, TheStep)
```

```
        String TheTable
        Variable TheStep
        Wave myXWave = WaveRefIndexed(TheTable,0,3)
        Variable index = 1
        Wave myYWave = WaveRefIndexed(TheTable,index,3)
        Make /O GateVals
        Make /O rdsVals
        Wave coef = W_coef   // coef is local name for W_coef
        Edit as "Fit Table"
        do
                Wave myYWave = WaveRefIndexed(TheTable, index, 3)
                if (!WaveExists(myYWave))
                        break
                endif
                CurveFit line myYWave /X=myXWave
                Duplicate /O W_coef, $("fit" + num2str((index-1)*TheStep))
                AppendtoTable $("fit" + num2str((index-1)*TheStep))
                GateVals[index - 1] = (index - 1)*TheStep
                rdsVals[index - 1] = 1/coef[1]
                index += 1
        while (WaveExists(myYWave))
        DeletePoints (index - 1),(128 - index + 1), GateVals, rdsVals
End
```

Section B.2 Flatten Data

The macro "Flatten" was used to subtract the gently sloping background signal from scans of the drain current I_D as a function of the charge-imaging FET position underneath a charged, metal SPM tip. The data from the scan is assumed to be in a square matrix, and the macro plots the original data, the sloping background, and the data with background subtracted. There are two inputs: "name", the name of the data matrix, and "axis", a choice of which points in the data matrix to fit the sloping background.

```
#pragma rtGlobals=1          // Use modern global access method.

Macro Flatten(name, axis)
// Purpose:     Takes a matrix called "name" and subtracts off a plane determined by
//              (0,0,name[0][0]), (0,0,name[size][size]), (0,0,name[size][0]) or
//              (0,0,name[0][0]), (0,0,name[size][size]), (0,0,name[0][size])
//              if the third option is set to "y"
//              Image plots the original, the fitted plane, and (orginal – fit)
//
// Assumes:             "name" is square, side length = size
//
String name, axis = "x"
//
        Prompt name, "Enter the wave name to be flattened: "
        Prompt axis, "Take third point along x or y-axis?  x is default; enter 'y' to set y-
axis: "
//
//      Plot the original data matrix
//
        Display/I/W=(1,1,4,4); AppendImage $name; DelayUpdate
        ModifyGraph swapXY=1, width=216, height=216
        Label bottom, "X"; DelayUpdate; Label left, "Y"
//
//      Now, compute the plane, which will be defined by   z = Ax + By + C
//
        WaveStats /Q $name
        Variable size = sqrt(V_npnts)
        Variable x0 = 0, y0 = 0, z0=$name[0][0]
        Variable x1 = size, y1 = size, z1 = $name[size][size]
        Variable x2 = size, y2 = 0, z2 = $name[size][0]
```

```
        if (stringmatch(axis,"y"))
                x2 = 0; y2 = size; z2 = $name[0][size]
        endif

        Variable denom = y0*(x2 - x1) - y1*(x2 - x0) + y2*(x1 - x0)
        Variable A =  -((y2-y1)*z0 - (y2-y0)*z1 + (y1-y0)*z2)/denom
        Variable B = ((x2-x1)*z0 - (x2-x0)*z1 + (x1-x0)*z2)/denom
        Variable C = -((x2*y1-x1*y2)*z0 - (x2*y0-x0*y2)*z1+(x1*y0-
x0*y1)*z1)/denom
//
// Now, generate and plot this plane
//
        Duplicate /O $name, $name+"_base"
        ComputePlane($name+"_base", A, B, C, size)

        Display/I/W=(1,5,4,8); AppendImage $name+"_base"; DelayUpdate
        ModifyGraph swapXY=1, width=216, height=216
        Label bottom, "X"; DelayUpdate; Label left, "Y"

// Now. subtract off the plane and

        Duplicate /O $name, $name+"_flat"
        $name+"_flat" -= $name+"_base"

        Display/I/W=(5,1,8,4); AppendImage $name+"_flat"; DelayUpdate
        ModifyGraph swapXY=1, width=216, height=216
        Label bottom, "X"; DelayUpdate; Label left, "Y"
end

Function ComputePlane(toplane, a, b, c, size)
// Purpose:             Computes the plane determined by z = a*x + b*y + c and stores the
results in
//                                  toplane.  size is the side length of toplane
//
Wave toplane
Variable a, b, c, size
Variable i = 0, j = 0   // looping indices
do
        do
                toplane[i][j] = a*i + b*j + c
                j += 1
        while (j < size)
        j = 0
        i += 1
while (i <size)
end
```

Section B.3 Peak Slicer

The macro "ScaledSlice45" plots a square matrix containing data from scans of the drain current I_D as a function of charge-imaging FET position underneath a charged, metal SPM tip. Two inputs are required: "w", the name of the data matrix, and "scaling", the number of nanometers in the side length of the data matrix.

```
#pragma rtGlobals=1          // Use modern global access method.

Function InitGlobal45()
// Purpose:     To set up all the global variables needed
//
        Variable /G ident45 = 0          // To index each time the slicer is run
                                         // so the waves are uniquely
        String /G uprx = "upright_x"  // Name stem of x wave for
                                         // low left to upper right line
        String /G upry = "upright_y"  // Name stem of y wave for
                                         // low left to upper right line
        String /G lowrx = "lowright_x" // Name stem of x wave for
                                           // upper left to low right line
        String /G lowry = "lowright_y" // Name stem of y wave for
                                           // upper left to low right line
        String /G uprname = "uprt_slice"   // Name stem of wave for ... upper right slice
        String /G lowrname = "lowrt_slice"  // Name stem of wave for ... low right slice
end

Macro ScaledSlice45(w,scaling,dummy)
// Purpose:             Call the slicing function on wave w, and apply the scaling factor
//                              scaling = factor to convert the array size of w into nm
//
String w
Variable scaling = 1
String dummy
//
        Prompt w, "Enter the wave name to be sliced: ", popup, WaveList("scan*",";","")
        Prompt scaling, "Enter the scaling factor (nm/array side length): "
        Prompt dummy, "Did you load the device file?"
//
        Slice45($w, scaling)
end

Function Filler45(w, scale)
```

```
// Purpose:              Fills the wave w such that w[i] = i*scale
//
Wave w
Variable scale
        WaveStats /Q w
        Variable F_index = 0
        do
                w[F_index] = F_index*scale
                F_index += 1
        while (F_index < V_npnts)
end

Function Slice45(w, sf)
Wave w
Variable sf
// Purpose:     Takes a matrix of data, finds the peak, take an x-slice, a y-slice, and fits
//                              these slices to Lorentzians
//
// Assumptions:         Data matrix w is square, there is a single peak in the data
//                              sf is the scaling factor that converts the data size to nm
        NVAR suffix45 = ident45
        SVAR urx = uprx
        SVAR ury = upry
        SVAR lrx = lowrx
        SVAR lry = lowry
        SVAR urslice = uprname
        SVAR lrslice = lowrname

        WaveStats /Q w   // WaveStats puts the location of Max[w], in V_maxloc
        Variable size = sqrt(V_npnts)   // size is the side length of the matrix
        Variable yindex = trunc(V_maxloc/size)  // yindex is the col. index of the y-slice
        Variable xindex = V_maxloc - (yindex * size)   // xindex is the row index
                                                        // of the x-slice
//
        Make /O/N=(size+1) $"axiswave"+num2str(suffix45)
        Filler45($"axiswave"+num2str(suffix45),sf)   // make an axis wave
//
        Display /I/W=(7,1,12,5);AppendImage w vs
{$"axiswave"+num2str(suffix45),$"axiswave"+num2str(suffix45)}
                ModifyGraph width=252,height=252;DelayUpdate   // Image plot the data
                SetAxis left 0, (size*sf);DelayUpdate
                Label left "X-axis (nm)";DelayUpdate
                SetAxis bottom 0, (size*sf);DelayUpdate
                Label bottom "Y-axis (nm)"
        AppendMatrixContour w vs
{$"axiswave"+num2str(suffix45),$"axiswave"+num2str(suffix45)}; DelayUpdate
```

```
        ModifyContour " labels=0,
ctablines={*,*,RedWhiteBlue,1},moreLevels=0,moreLevels={str2num(num2str((V_max
+ V_min)/2))}
String holder = NameOfWave(w)+"="+num2str((V_max+V_min)/2)
        ModifyGraph lsize($"'"+holder+"'")=2,rgb($"'"+holder+"'")=(65535,65535,0)
        if (xindex < yindex)
        // execute if condition is true
                Make /O/N=2 $urx+num2str(suffix45) = {0,(size - (yindex - xindex))*sf}
                Make /O/N=2 $ury+num2str(suffix45) = {(yindex - xindex)*sf, size*sf}
        else
        // execute if condition is false
                Make /O/N=2 $urx+num2str(suffix45) = {(xindex - yindex)*sf, size*sf}
                Make /O/N=2 $ury+num2str(suffix45) = {0,( size - (xindex - yindex))*sf}
        endif

        if (xindex + yindex < size)
                Make /O/N=2 $lrx+num2str(suffix45) = {0, (xindex + yindex)*sf}
                Make /O/N=2 $lry+num2str(suffix45) = {(xindex + yindex)*sf, 0}
        else
                Make /O/N=2 $lrx+num2str(suffix45) = {(xindex + yindex - size)*sf,
size*sf}
                Make /O/N=2 $lry+num2str(suffix45) = {size*sf,(xindex + yindex -
size)*sf}
        endif

// Draw the red lines showing the low left to upper right and low right to upper left slices

                AppendToGraph $ury+num2str(suffix45) vs $urx+num2str(suffix45)
                AppendToGraph $lry+num2str(suffix45) vs $lrx+num2str(suffix45)
//
//  Okay, now add in the lines showing the device features in blue at thickness 2
//      Assumed: we have already loaded in the waves from device_features.awav
//                          whose wave names are specified in InitGlobal()
//
// Make local names for the device feature waves
//
        Wave cyl = channely
        Wave cxl = channelx
        Wave gyl = gatey
        Wave gxl = gatex
        Wave eyl = etchy
        Wave exl = etchx
//
// Now, make local *waves* for the device feature waves
//
        Make $"cy"+num2str(suffix45) = cyl*sf
```

```
		Make $"cx"+num2str(suffix45) = cxl*sf
		Make $"gy"+num2str(suffix45) = gyl*sf
		Make $"gx"+num2str(suffix45) = gxl*sf
		Make $"ey"+num2str(suffix45) = eyl*sf
		Make $"ex"+num2str(suffix45) = exl*sf

		AppendToGraph $"cy"+num2str(suffix45) vs
$"cx"+num2str(suffix45);DelayUpdate
		ModifyGraph
lsize($"cy"+num2str(suffix45))=2,rgb($"cy"+num2str(suffix45))=(0,0,65535)
		AppendToGraph $"gy"+num2str(suffix45) vs
$"gx"+num2str(suffix45);DelayUpdate
		ModifyGraph
lsize($"gy"+num2str(suffix45))=2,rgb($"gy"+num2str(suffix45))=(0,0,65535)
		AppendToGraph $"ey"+num2str(suffix45) vs
$"ex"+num2str(suffix45);DelayUpdate
		ModifyGraph
lsize($"ey"+num2str(suffix45))=2,rgb($"ey"+num2str(suffix45))=(0,0,65535)

//
//		Now, swap the axes to get the correct orientation
//
		ModifyGraph swapXY=1

//		Temporary variable to store fitting results
		Wave coef = W_coef
//
		Variable ursize = size - abs(yindex - xindex) + 1
		Make /O/N=(ursize) dopppelg, $"uraxiswave"+num2str(suffix45)
		Filler45($"uraxiswave"+num2str(suffix45), sf*sqrt(2))

		Variable urcounter = max(0, xindex - yindex), urindex = 0

		if (xindex < yindex)
			do
				dopppelg[urcounter] = w[urcounter][yindex - xindex + urcounter]
				urcounter += 1
			while (urcounter <= size - (yindex - xindex))
		else
			do
				dopppelg[urindex] = w[urcounter][urcounter - (xindex - yindex)]
				urcounter += 1
				urindex += 1
			while (urcounter <= size)
		endif
```

```
        Duplicate /O dopppelg, $urslice+num2str(suffix45)

        KillWaves doppelg

// now plot and fit the lower left -> upper right slice

        Display /I/W=(1,1,6,4) $urslice+num2str(suffix45) vs
$"uraxiswave"+num2str(suffix45)
        CurveFit /Q/N/L=(ursize) lor $urslice+num2str(suffix45) /X =
$"uraxiswave"+num2str(suffix45) /D;DelayUpdate
        ModifyGraph rgb($"fit_"+urslice+num2str(suffix45))=(0,0,0);DelayUpdate
// curve fit urslice and show it in black
        Legend /A=MC/X=-25/Y=40f;DelayUpdate
        Textbox /F=1 "FWHM = "+num2str(2*sqrt(coef[3]))+" nm";DelayUpdate
        Label bottom "nm";DelayUpdate

        Variable lrsize
        if (xindex + yindex < size)
                lrsize = yindex + xindex + 1
        else
                lrsize = (2*size) - yindex - xindex
        endif

                Make /O/N=(lrsize) doppelg, $"lraxiswave"+num2str(suffix45)
                Filler45($"lraxiswave"+num2str(suffix45), sf*sqrt(2))  // sqrt(2) for going
along diag.

                Variable lrindex = 0

        if (xindex + yindex < size)
                do
                        doppelg[lrindex] = w[lrindex][lrsize - 1 - lrindex]
                        lrindex += 1
                while (lrindex < lrsize)
        else
                do
                        doppelg[lrindex] = w[xindex + yindex -size + lrindex][size -
lrindex]
                        lrindex += 1
                while (lrindex < lrsize)
        endif

        Duplicate /O doppelg, $lrslice+num2str(suffix45)

// do and plot the lrslice
```

```
        Display /I/W=(1,5,6,8) $lrslice+num2str(suffix45) vs
$"lraxiswave"+num2str(suffix45)
        CurveFit /Q/N/L=(lrsize) lor $lrslice+num2str(suffix45)
/X=$"lraxiswave"+num2str(suffix45) /D;DelayUpdate
        ModifyGraph rgb($"fit_"+lrslice+num2str(suffix45))=(0,0,0);DelayUpdate
 // curve fit yslice and show it in black
        Legend /A=MC/X=-25/Y=40;DelayUpdate
        Textbox /F=1 "FWHM = "+num2str(2*sqrt(coef[3]))+" nm"
        Label bottom "nm"

        suffix45 += 1
end
```

Appendix C Suppliers

This appendix details a list of all of the suppliers I have used during my tenure at Harvard. It is meant to aid future students by saving them the trouble of wading through countless "yellow slips" and to save Ralph Generazzo the trouble of correcting generations of future students for putting down incorrect item numbers.[50] The abbreviation in parentheses after the company name is used for reference in the main body of this thesis. The items in brackets are what is typically ordered from the company.

Alfa Aesar Inc. (AAI) [metals for evaporation]

Allied Electronics, Inc. (AEI) [electrical connectors and wires]

Apple Store for Education (ASE) [Macintosh computers and peripherals]
800.800.2775 (tel)

Doe & Ingalls (D&I) [semiconductor grade acetone, methanol, and isopropyl alcohol]
391.0090 (tel)

Fluoroware Inc. (FWI) [anti-static tweezers and sample boxes]
3500 Lyman Boulevard
Chaska, Minnesota 55318
800.394.4083 (tel)
800.763.5820 (fax)

G. Finkenbeiner (GFB) [6" diam., 1/2" thick polished quartz windows for the ion miller]
33 Rumford Ave.
Waltham, MA
781.899.3138 (tel)

IGO (IGO) [ultra-high purity nitrogen gas, forming gas]

[50] Area codes are, of course, subject to the whims of the current telephone concern, which will probably be one company again soon.

Infrared Laboratories (IRL) [custom liquid He Dewars and assorted parts]
1808 E. 17th Street
Tucson, AZ 85719
520.622.7074 (tel)
520.623.0765 (fax)

Janis Research Corp. (JRC) [liquid He transfer tubes and attachments]
2 Jewel Drive
P.O. Box 696
Wilmington, MA 01887
978.657.8650 (tel)
978.658.0349 (fax)

LabSafety Supplies (LSS) [HF safety clothing]
P.O. Box 1368
Janesville, WI 53547
800.356.0783 (tel)

Lakeshore Cryotronics, Inc. (LCI) [diode thermometers, Dewar widgets]
575 McCorkle Blvd.
Westerville, OH 43082
614.891.2244 (tel)
614.818.1600 (fax)

MacWarehouse (MWH) [Macintosh software and media]
800.696.1727 x7103 (tel)

McMaster Carr (MMC) [everything from organizing bins to screws]
732.329.3200 (tel)

MDC Vacuum Products Corp. (MDC) [vacuum supplies: flanges, O-rings, ...]
23842 Cabot Blvd.
Hayward, CA 94545
800.443.8817 (tel)
510.887.0626 (fax)

MedTech (MTI) [liquid carbon dioxide cylinders]
781.395.1946 (tel)
781.395.9095 (fax)

MicroChem Corp. (MCC) [PMMA, anisole]
1254 Chestnut Street
Newton, MA 02464
617.965.5511 (tel)
617.965.5818 (fax)

MicroTech Inc. (MCT) [micro-connectors]
1420 Conchester Highway
Boothwyn, PA 19061
610.459.3566 (tel)

Millipore (MLP) [air gun and filters for ultra-high purity nitrogen]
80 Ashby Road
Bedford, MA 01730
800.645.5476 (tel)
781.533.3110 (fax)

Newark Electronics (NEI) [electronics components: batteries, ICs, ...]
978.551.4300 (tel)

R. D. Mathis (RDM) [thermal evaporator tungsten boats and Cr rods]
2840 Gundry Avenue
Long Beach, CA 90806
310.426.7049 (tel)

Semiconductor Packaging Materials, Inc. (SPM) [Au-wire for wirebonding]
1 Labriola Court
Armonk, NY 10504
914.273.5500 (tel)
914.273.2005 (fax)

Structure Probe, Inc. (SPI) [C-, Ag-paint and thinners]
P.O. Box 656
West Chester, PA 19381
610.436.5400 (tel)

Tousimis Research Corporation (TRC) [critical point dryer and supplies]
P.O. Box 2189
Rockville, MD 20847
800.638.9558 (tel)

VWR (VWR) [general lab supplies]
800.234.9300 (tel)

Wavemetrics, Inc. (WMI) [IGOR Pro Data Analysis Program]
P.O.Box 2088
Lake Oswego, OR 97035
503.620.3001 (tel)
503.620.6754 (fax)