

# Cryogenic field-effect transistor with single electronic charge sensitivity

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We have fabricated matched pairs of cryogenic field-effect transistors with input charge sensitivity  $q_n=0.01 e/\sqrt{\text{Hz}}$  at  $T=1.3$  K, low input capacitance 0.4 pF, and extremely high input resistance in excess of  $10^{15} \Omega$ . Low leakage permits dc charge-coupled operation for times up to  $\sim 10^3$  s. The channel noise is characterized by a flat spectrum at high frequencies, and  $1/f$  noise below a corner frequency  $f_c < 1$  kHz. These devices can resolve charge differences as small as  $q_n \sqrt{f_c} = 0.4e$ .

The study of electrons in mesoscopic semiconductor structures has proven to be very interesting, both for physics and for possible device applications. Sensitive capacitive measurements of nanostructures, recently demonstrated by the detection of single electrons in single quantum states<sup>1</sup> and quantum dots<sup>2,3</sup> can be useful tools to study the nature of electron states and transport.<sup>4,5</sup> The Coulomb blockade<sup>6</sup> has been exploited in devices and circuits controlled by single-electronic charges;<sup>7-9</sup> it also provides the basis of operation of single-electron transistors (SET's) with charge sensitivity much less than  $e$ . For possible applications of single electronics, it is necessary to have impedance converting devices capable of sensing transitions of a single-electronic charge while providing fan out and driving lower impedance lines.

In this letter we describe cryogenic field-effect transistors (FET's) with low charge noise  $0.01 e/\sqrt{\text{Hz}}$ , very low  $1/f$  noise, and charge resolution  $0.4e$ , less than a single electronic charge. In contrast to SETs based on the Coulomb blockade,<sup>7,10-12</sup> our devices are simply small conventional FETs. Cryogenic FETs have significant advantages over SETs: simple fabrication, robustness, large dynamic range, and a well-established principle of operation. They single-electron charge transitions while driving low impedance loads. To reduce input capacitance and permit sensitive charge-coupled measurements, cryogenic FETs can be fabricated on the same chip as the nanostructure under study. This is a first step toward nanostructure integrated circuits. While the charge sensitivity of our FETs is not as great as that attainable with the best SETs,<sup>13-15</sup> it greatly exceeds that of conventional electrometers and permits a wide range of novel experiments. The power dissipation is less than  $1 \mu\text{W}$ , making them suitable for use in dilution refrigerators, although temperatures below 1 K are not required.

Our devices are fabricated from a GaAs/Al<sub>0.3</sub>Ga<sub>0.7</sub>As heterostructure with a near-surface ( $d=520 \text{ \AA}$ ) two-dimensional electron gas (2DEG) with sheet density  $n_s=2.6 \times 10^{11} \text{ cm}^{-2}$  and mobility  $\mu=2.0 \times 10^5 \text{ cm}^2/\text{V s}$ . Figure 1 is a top view of a matched pair of devices. The source-drain channels are vertical in the photograph and are defined using electron beam lithography and a mesa etch. Each channel is  $60 \mu\text{m}$  long and  $3 \mu\text{m}$  wide. The length is chosen to be much longer than the mean-free path  $\ell=2 \mu\text{m}$  so that transport along the channel is diffusive, and the aspect ratio of the

channel is chosen to give a relatively large resistance  $R_{\text{DS}} \sim 2 \text{ k}\Omega$ . Metal gates are deposited by thermal evaporation of  $200 \text{ \AA}$  Cr and  $2000 \text{ \AA}$  Au. Ohmic contacts to the 2DEG are achieved by thermal diffusion of In pressed onto the chip surface.

Low-temperature electrical measurements are made by immersing the FET samples in pumped liquid He. Data are taken using a four-probe arrangement, with shielded twisted pairs used throughout. The channel is current biased using a low-noise voltage source in series with a large resistance, typically  $1 \text{ M}\Omega$ , and the drain-to-source voltage,  $V_{\text{DS}}$  is amplified using either a PAR 117 or a PAR 118 low-noise differential preamplifier. The measured input noise  $e_n$  and  $i_n$  above 100 Hz is less than  $4.7 \text{ nV}/\sqrt{\text{Hz}}$  and  $850 \text{ fA}/\sqrt{\text{Hz}}$  for the 117 and  $1.2 \text{ nV}/\sqrt{\text{Hz}}$  and  $1200 \text{ fA}/\sqrt{\text{Hz}}$  for the 118. To isolate the FET from radio frequency radiation, all data are taken inside a shielded room and cooled metal film resistors with  $R_i=909 \Omega$  are inserted in each lead.

The measured dc performance of a single FET at  $T=4.2$  K is shown in Fig. 2. As shown in Fig. 2(a), the shape of the measured source-drain characteristics resembles those for room-temperature FETs, but the range of drain-to-source voltage  $V_{\text{DS}}$  is much smaller. As  $V_{\text{DS}}$  is increased, we observe breakdown due to carrier heating at  $V_{\text{DS}} \sim 70$  to  $100 \text{ mV}$ , which limits the useful bias current. Figure 2(b) is a plot of the channel conductance  $G$  versus gate voltage  $V_G$  using small drain currents for which  $V_{\text{DS}} < V_G$ . As shown, the channel pinches off smoothly; the measured threshold

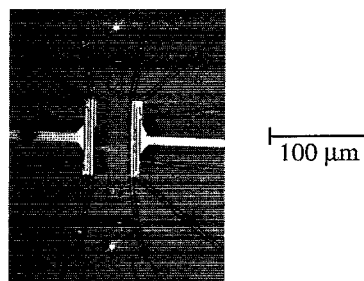


FIG. 1. Top view of two transistors. The source-drain channels are vertical and centered in the photograph. The light areas are gates. The scale is indicated by the bar at the right.

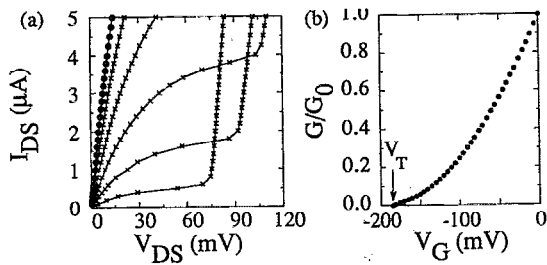


FIG. 2. (a) Family of source-drain characteristics taken at  $T=4.2$  K for  $V_g=0$  mV (dots),  $-30$ ,  $-60$ ,  $-90$ ,  $-120$ , and  $-150$  mV. The lines are guides to the eye. (b) Cutoff graph of conductance  $G$ , normalized by its value  $G_0=R_{DS}^{-1}=0.415$  mS at zero gate bias. The cutoff threshold  $V_T=-0.185$  V is indicated by the arrow.

$V_T=-0.185$  V. This threshold is at least an order of magnitude smaller than those for conventional devices, due to the low values of  $n_s$  and  $d$ .

The input of the cryogenic FET can be modeled as an input capacitance  $C_{in}$  in parallel with a large resistance  $R_{in}$  due to leakage and the effects of traps. The measured input capacitance is  $C_{in}=0.37$  pF, which agrees well with the value  $0.40$  pF estimated from the depth  $d=520$  Å of the 2DEG and the nominal area  $180$   $\mu\text{m}^2$ . At low temperatures,  $R_{in}$  is extremely large, permitting charge-coupled measurements over long times. We attempted to measure  $R_{in}$  at  $T=4.2$  K by inserting a cooled 1-pF mica capacitor in series with the gate, adjacent to the device. The response of this circuit to a step in  $V_G$  is characterized by an exponential decay with time constant  $\tau=R_{\Sigma}C_{\Sigma}$ , where  $R_{\Sigma}=R_{in}||R_{mica}$  and the total capacitance is  $C_{\Sigma}=C_{mica}+C_{in}+C_{stray}<2$  pF. Since  $\tau$  is measured to be  $>2\times 10^3$  s,  $R_{in}>R_{\Sigma}\sim 10^{15}$   $\Omega$ . Thus cryogenic FETs can operate in the charge-coupled regime for times up to  $\sim 1000$  s.

The small signal ac response of the sample with  $V_G=-20$  mV and  $I_D=100$  nA is shown in Fig. 3. The device from which this data was taken is fabricated on the same chip as the FET used for Fig. 2, and has similar characteristics. The signal gain is expressible as an inverse capacitance or "transelastance"  $C_A^{-1}=|v_d/q_g|$ , where  $v_d$  is the small signal voltage measured at the output and  $q_g$  is the corresponding small signal charge on the gate. The dimensionless gain  $A=C_{in}C_A^{-1}=|v_d/v_g|$  is plotted in Fig. 3, where  $v_g$  is the small signal gate voltage. As shown, the graph of  $A$  vs  $f$  is flat over a wide frequency range, limited at high frequencies in Fig. 3 by the cable capacitance and the source resistance.

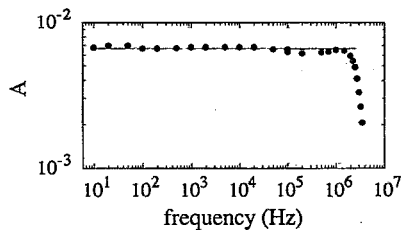


FIG. 3. Dimensionless gain  $A=C_{in}C_A^{-1}$  measured with  $T=4.2$  K and  $I_D=100$  nA. Both axes are logarithmic. The rolloff above 2 MHz is due to cable capacitance. The horizontal line is a guide to the eye.

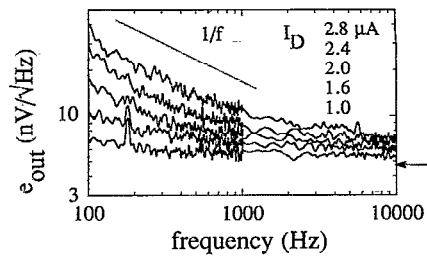


FIG. 4. Noise spectra of the FET output, with  $T=1.3$  K and  $V_G=-90$  mV, for  $I_D=1.0, 1.6, 2.0, 2.4,$  and  $2.8$   $\mu\text{A}$ . The line has the slope appropriate for  $1/f$  noise. The arrow at the right indicates the noise level of the preamplifier. The small feature at 180 Hz is due to magnetic pickup and is ignored in determining  $f_c$ .

In the variable resistance regime,  $C_A^{-1}$  is proportional to  $I_D$ .

Measured noise power spectra at  $T=1.3$  K and  $V_G=-90$  mV are plotted in Fig. 4 for several values of  $I_D$ . The measured voltage noise  $e_n=4.7$  nV/ $\sqrt{\text{Hz}}$  of the preamplifier is significant, and is indicated by the arrow at the right of Fig. 4; over the frequency range shown  $e_n$  is spectrally flat ( $i_n$  makes a negligible contribution above 200 Hz for this source resistance). The additional noise, attributed to the FET, consists of  $1/f$  noise superimposed upon a white background, as shown. The two intersect at a corner frequency  $f_c$  that increases with  $I_D$ . The white noise level  $e_{\text{FET}}$  associated with the FET is generally smaller than that of the preamplifier. Subtraction of the preamplifier contribution from the measured spectrum gives  $e_{\text{FET}}^2=e_{\text{out}}^2-e_n^2-[i_n(R_{DS}+2R_i)]^2$ .

Figure 5 shows the measured white noise level expressed in drain to source voltage [Fig. 5(a)] and in terms of charge on the gate [Fig. 5(b)], as well as the measured corner fre-

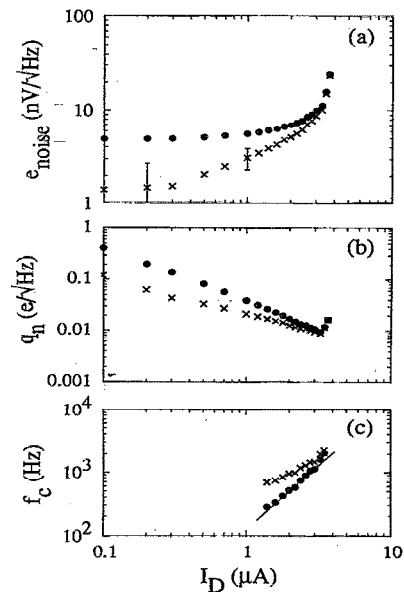


FIG. 5. (a) Noise levels  $e_{\text{out}}$  (dots) and  $e_{\text{FET}}$  (crosses) vs  $I_D$  as measured with  $T=1.3$  K and  $V_G=-90$  mV. (b) Charge sensitivity vs  $I_D$ , as determined from the noise levels in (a). (c) Corner frequency  $f_c$  vs  $I_D$ . The line has slope = 2. All axes are logarithmic and the abscissas are the same in (a), (b), and (c).

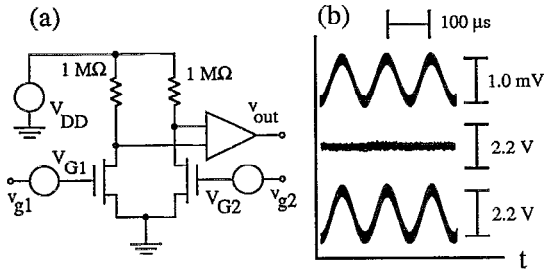


FIG. 6. (a) Differential amplifier circuit. (b) The top trace is the gate drive. The middle trace shows  $v_{out}$  for the drive applied to only the noninverting input. Scales are indicated at the top and right of the figure. The numerical values for the circuit parameters are  $V_{G1} = -0.133$  V, and  $V_{G2} = -0.148$  V, and  $V_{DS} = 0.100$  V. The external preamplifier gain is  $10^5$ .

quency for  $1/f$  noise [Fig. 5(c)]; all data were taken at  $T = 1.3$  K with  $V_G = -90$  mV. The measured total white noise level  $e_{out}$  (dots) and the contribution  $e_{FET}$  from the device alone (crosses) are both plotted in Fig. 5(a) as a function of  $I_D$ . For small drain currents,  $e_{FET} < 2$  nV/ $\sqrt{\text{Hz}}$ ; this level corresponds to a noise temperature  $T_n < 9$  K. Although the noise increases with  $I_D$ , the gain increases more strongly, and the overall charge sensitivity  $q_n = e_{noise} C_{in}/A = e_{noise} C_A$  improves with drain current. The charge sensitivity  $q_n$  is plotted in Fig. 5(b) including preamplifier noise ( $e_{noise} = e_{out}$ ) and for the FET alone ( $e_{noise} = e_{FET}$ ). As shown, the sensitivity can be well below  $0.1$  e/ $\sqrt{\text{Hz}}$  and improves with  $I_D$ . The greatest sensitivity of  $1.0 \times 10^{-2}$  e/ $\sqrt{\text{Hz}}$  is obtained for relatively large drain current  $I_D = 3.3$   $\mu\text{A}$ , just below breakdown at  $3.5$   $\mu\text{A}$ . At this drain current  $e_{out}$  is determined by the FET rather than the preamplifier. As  $I_D$  is increased into the breakdown regime,  $e_{noise}$  and  $q_n$  rise rapidly as shown in Figs. 5(a) and 5(b). The corner frequency  $f_c$  is plotted versus  $I_D$  in Fig. 5(c) both including preamplifier noise (dots) and for the FET alone (crosses). For drain currents which give the best charge sensitivity,  $f_c \sim 1$  kHz, a factor  $\sim 100$  lower than the best commercially available GaAs transistors.<sup>16</sup> For the case in which  $e_n$  dominates  $e_{out}$  and the white noise level is essentially fixed,  $f_c$  increases approximately quadratically with  $I_D$ , as shown in Fig. 5(c). This is consistent with the idea that  $1/f$  noise occurs as a fluctuation  $\delta R$  in resistance.<sup>17,18</sup> for which the noise voltage is  $I_D \delta R$ .

The charge resolution  $Q_f = q_n \sqrt{f_c}$  describes the smallest change in gate charge that can be measured in the presence of  $1/f$  noise, because time averaging improves charge sensitivity only for white noise. For these cryogenic FETs  $Q_f$  is approximately independent of  $I_D$  below breakdown; at  $T = 1.3$  K the charge resolution is  $Q_f = 2.2e$  for  $V_G = 0$  V and  $Q_f = 0.4e$  for  $V_G = -90$  mV. Thus we can resolve single electronic charges at kHz rates in simple charge circuits without resorting to lock-in techniques. Devices of this type are particularly well suited to charge-coupled measurements of

semiconductor nanostructures, because the size and location of the FET can be optimized without constraints imposed by lead capacitance.

In Fig. 6(a) we show a simple differential amplifier circuit constructed from two FETs fabricated on the same wafer. The source-drain resistances of this pair are matched to within 1% at  $V_G = 0$ . As  $V_G$  is decreased, the matching degrades slightly, but the freedom in setting  $V_G$  and  $I_D$  allows us to equalize  $\Delta R_{DS}/\Delta V_G$ . In the top trace of Fig. 6(b) we show a sinusoidal drive signal of amplitude 1 mV  $p-p$  and frequency 10 kHz. In the lower two traces of Fig. 6(b) we show the preamplifier output  $v_{out}$  for drive applied to both inputs, and for drive applied to only the noninverting input. The measured common mode rejection ratio of this circuit is 40 dB. It is clear that similar devices can be combined to form multitransistor cryogenic circuits that could serve as amplifiers with high charge sensitivity.

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