

Charge-imaging field-effect transistor

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Charge-imaging field-effect transistors (FETs) were fabricated from a GaAs/AlGaAs heterostructure containing a near-surface two-dimensional electron gas. These FETs have quantum point contact geometries to minimize the size of the channel and to improve the spatial resolution. The charge noise at $T=4.2$ K has a $1/f$ behavior and reaches values $\ll 1 e/\text{Hz}^{1/2}$ at 30 kHz. The spatial resolution of the FET was measured at liquid He temperatures using a scanned probe microscope with a charged tip. The charge sensitivity of the FET is confined to a disk with full width at half maximum 340 nm. These FETs are suitable for integration onto a GaAs/AlGaAs scanned probe microscopy cantilever. © 2001 American Institute of Physics. [DOI: 10.1063/1.1395516]

Two-dimensional electron gas (2DEG) systems provide a means by which to explore quantum phenomena in small structures.^{1,2} Scanned probe microscopy (SPM) techniques are being developed to image the spatial distribution and flow of electrons.^{3–9} A charge-imaging field-effect transistor (FET) with high spatial resolution can be placed on a SPM cantilever to image the charge distribution directly. Field-effect transistors provide power gain for sensitive imaging, and they are well suited for miniaturization, which increases their sensitivity and spatial resolution.^{10,11}

In this letter, we describe a charge-imaging FET fabricated from a GaAs/AlGaAs heterostructure. Integrated strain-sensing cantilevers for scanned probe microscopy have been constructed from a GaAs/AlGaAs heterostructure containing a quantum well by placing a strain-sensing FET at the cantilever base.^{10,11} A charge-imaging FET placed at the tip of the cantilever could image charge distributions. The charge-imaging FET in the present work was constructed with a quantum point contact geometry to minimize the size of its channel and its capacitance to ground. The spatial resolution of the FET was imaged using a separate scanned probe microscope with a charged tip at liquid He temperatures. These FETs have several advantages as charge imagers: a small channel area for high spatial resolution, high charge sensitivity ($\ll 1 e/\text{Hz}^{1/2}$), and low power dissipation ($< 10 \mu\text{W}$), which makes them suitable for heat-sensitive applications, including measurements at low temperatures in He dilution refrigerators.

The GaAs/AlGaAs heterostructure used to make these charge-sensing FETs was designed to make free-standing SPM cantilevers. A GaAs quantum well is doped from both sides by two Si δ -doping layers; GaAs cap layers are located on both sides of the quantum well for use on a free-standing cantilever. The sequence of layers is 8000 Å of $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}$, 100 Å of GaAs (cap layer), 1510 Å of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$, a Si δ -doping layer, 220 Å of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$, 200 Å of GaAs

(quantum well), 220 Å of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$, a second Si δ -doping layer, 250 Å of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$, and 50 Å of GaAs (cap layer). The 2DEG sheet density $n_s = 8.7 \times 10^{11} \text{ cm}^{-2}$ was obtained from Shubnikov–de Haas measurements of the magnetoresistance at $T=20$ mK in the dark.

Figure 1(a) is a scanning electron micrograph of the charge-imaging FET. The dark regions are etch trenches, where the 2DEG is permanently depleted, and the bright feature is a metal gate. The charge-imaging FET is designed for integration onto a GaAs/AlGaAs SPM cantilever, and the V-shaped etch trench at the top of Fig. 1(a) defines the outer edge of a SPM cantilever and one side of the FET channel. The FET gate defines the other side of the channel. The etch trench next to the gate in Fig. 1(a) minimizes leakage currents underneath the gate. Figure 1(b) is a schematic diagram showing how the FET channel is formed between the gate and the V-shaped etch trench.

The FET was fabricated using the following process. The FET etch trenches and gate were formed using electron-beam lithography. The trenches were defined by dry etching an exposed pattern of polymethylmethacrylate (PMMA) with a directed Ar ion-beam system. The metal gate was fabricated by the lift-off technique with a new bilayer of PMMA by thermally evaporating 5 nm of Cr, followed by 40 nm of Au. The minimum lithographic distance between the gate

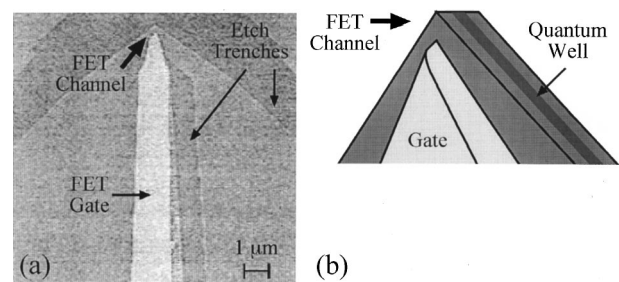


FIG. 1. (a) Scanning electron micrograph of the charge-imaging FET. The darker, gray regions are etch trenches, and the bright feature is the metal gate. (b) Schematic diagram of the FET's location.

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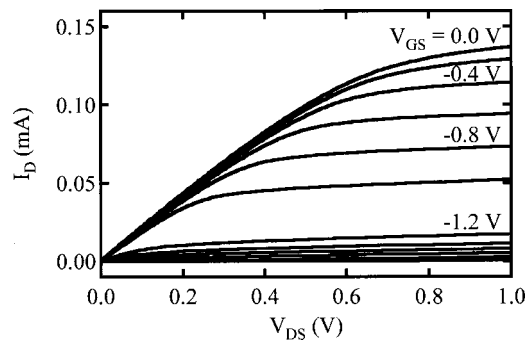


FIG. 2. Drain characteristics of the FET at $T=4.2$ K. The drain current I_D is plotted as a function of the drain-to-source voltage V_{DS} for a series of gate-to-source voltages V_{GS} , spaced by -0.2 V, which begin at 0.0 V (top curve) and end at -2.2 V (bottom curve). The labels are the values of V_{GS} for the curve underneath the label. The drain current smoothly saturates below $V_{DS}=+1.0$ V, a voltage smaller than most commercial FETs.

and the V-shaped etch trench [see Fig. 1(a)] is 250 nm. Ohmic contacts to the 2DEG at the source and drain were formed far from the channel by annealed Ni:Au:Ge pads. Measurements of the FET characteristics were made at liquid He temperatures using low noise electronics including a PAR 124A lock-in amplifier and an HP 3561A spectrum analyzer.

Figure 2 plots the drain characteristics of the FET—drain current I_D versus drain-to-source voltage V_{DS} at $T=4.2$ K for a series of gate-to-source voltages V_{GS} . The values of V_{DS} shown are sufficient to bring the FET out of the quantum regime, and the drain characteristics are those of a conventional FET: the current I_D saturates as V_{DS} increases and is controlled by V_{GS} . The FET channel is formed for $V_{GS} < -0.8$ V when the 2DEG underneath the gate is depleted, as determined from a plot of conductance versus gate-to-source voltage. To use the FET as a charge imager, the operating point is set in the current saturation region of the drain characteristics. A nearby charged object then acts as a second gate, shifting I_D by an amount proportional to the external charge. The measured transconductance $g_m \approx 20 \mu\text{S}$, and the small signal drain-to-source resistance $r_{ds} \geq 200 \text{ k}\Omega$ for $V_{DS}=+1.0$ V and $V_{GS}=-1.0$ V. The frequency response was flat up to 30 kHz, the limit of our measurements, but the FET should respond at much higher frequencies.

To probe the charge sensitivity and spatial resolution of the FET, we used a cooled SPM.³ The SPM was cooled to 4.2 K by the cold plate of a liquid He dewar and surrounded by liquid He cooled radiation shields. The position of the FET was scanned underneath a metal-coated SPM tip using a piezoelectric tube. We charged the metal-coated tip by applying a dc voltage of -1.0 V between the tip and the channel. In this way, the tip acts as a charged second gate which capacitively couples to the FET channel, changing the drain current by ΔI_D . To image the charge sensitivity of the FET, the drain-to source-voltage was fixed at $V_{DS}=+1.0$ V, and the induced change in drain current ΔI_D was measured as the FET was scanned below the tip, which was held 100 nm above the surface.

Figures 3(a)–3(d) show images of the FET response ΔI_D versus tip position over a $6.6 \times 6.6 \mu\text{m}$ region. The pattern of the FET gate and etch trenches from Fig. 1(a) is shown by the yellow lines in Fig. 3. The color scale for ΔI_D has been

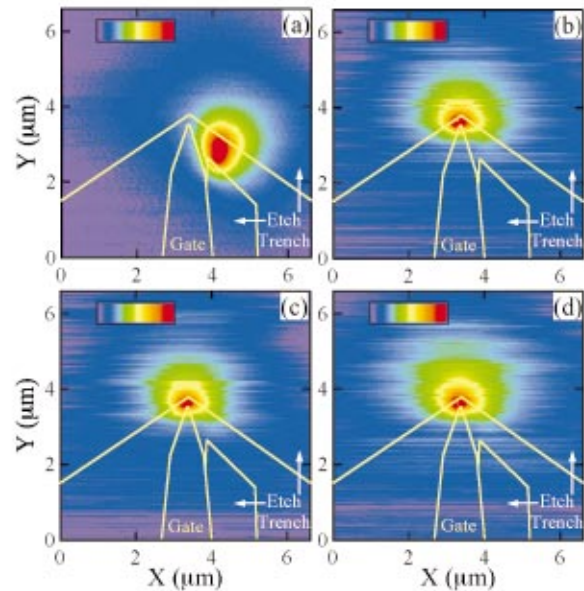


FIG. 3. (Color) Images of charge response obtained at $T=4.2$ K by scanning the charge-imaging FET under a charged scanned probe microscope tip. The FET was biased at $V_{DS}=+1.0$ V. The yellow lines outline the pattern of the FET gate and etch trenches. Each image shows the percentage change in the drain current ΔI_D induced by the charged scanned probe microscope tip. The color scale for each scan was chosen so that the half maximum is yellow at the center of the color scale. Purple corresponds to a minimum response of $\Delta I_D=0\%$, and red corresponds to maximum responses of ΔI_D (a) 2.4% , (b) 15.2% , (c) 17.5% , and (d) 19.6% . Gate-to-source voltages V_{GS} (a) 0.0 , (b) -0.9 , (c) -1.0 , and (d) -1.1 V.

chosen so that the half maximum is yellow at the center of the color scale; the spatial resolution and angular dependence of the FETs charge sensitivity are given by the yellow contours in the images. A gently sloping background signal was subtracted from these images.

Figures 3(a)–3(d) image the charge response of the FET for a series of gate-to-source voltages: $V_{GS}=0.0, -0.9, -1.0$ and -1.1 V, respectively. In Fig. 3(a), the gate is grounded to the source contact at the right of the image, and the etch trenches alone define a broad conduction channel 900 nm wide, and the response ΔI_D is a relatively small percentage of I_D . In Fig. 3(b), V_{GS} is sufficient to deplete the 2DEG underneath the gate and form a narrow FET channel between the gate and the V-shaped etch trench at the top in Figs. 3(a)–3(d); the lithographic width of the FET channel is 250 nm. The existence of this narrow channel is confirmed by the new location of the response peak in Fig. 3(b). In Figs. 3(c) and 3(d), V_{GS} is made more negative, further narrowing the channel and the area of charge response, and increasing the response ΔI_D as a percentage of I_D .

To quantify the spatial resolution of the charge-imaging FET, we use the full width at half maximum (FWHM) of the response peaks in Figs. 3(a)–3(d). Previous work⁵ has shown that the charged tip induces a Lorentzian-shaped change in 2DEG sheet density beneath the tip with FWHM equal to twice the spacing between the tip and the 2DEG, and that the FWHM varies little with the radius of curvature of the tip. To obtain the spatial resolution Δr of the FET alone, a Lorentzian of FWHM 300 nm was deconvolved from Figs. 3(a)–3(d), corresponding to tip to 2DEG spacing of 150 nm. For Fig. 3(b) we obtain $\Delta r=340$ nm, comparable to the litho-

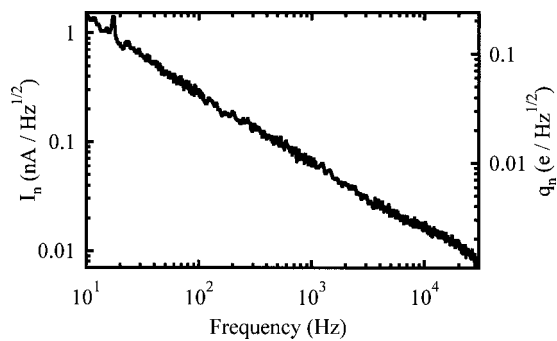


FIG. 4. Noise spectrum for the charge-imaging FET. The left vertical axis shows the current noise I_n , and the right vertical axis shows the charge noise q_n induced in the FET channel in units of electron charge $e/\text{Hz}^{1/2}$.

graphic distance 250 nm between the gate and the etch trench.

To estimate the amount of charge imaged by the FET, a simple model was used. The tip and FET channel were considered to be spheres separated by two dielectric layers,¹² an analytically soluble problem.^{13,14} The capacitance between the tip and the channel is then ~ 10 aF when the tip is directly over the channel at the height of 100 nm used to record the data for Fig. 3. For tip-to-channel voltage of -1.0 V, this capacitance gives an induced charge of $\sim 60 e$ in the FET channel.

Figure 4 shows the current noise spectrum of the charge-imaging FET. The noise at 4.2 K exhibits $1/f$ behavior and reaches ~ 50 pA/Hz^{1/2} at 30 kHz. To record these data the bias voltage was fixed at $V_{DS} = +1.0$ V, the gate voltage $V_{GS} = -1.1$ V, and the current noise spectrum was measured by an Ithaco 1211 preamplifier and an HP 3561A spectrum analyzer. The noise spectrum for charge induced in the FET channel is $q_n = I_n C_{gc} / g_m$, where C_{gc} is the capacitance between the gate and the channel and g_m is the transconductance. The capacitance C_{gc} is difficult to calculate, but modeling the channel as a sphere with radius of 340 nm (spatial resolution Δr of the response) gives $C_{gc} \sim 500$ aF. With this capacitance, the FET charge noise $q_n = 1.5 \times 10^{-3} e/\text{Hz}^{1/2}$ at 30 kHz.

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¹²To estimate the tip-channel capacitance, the tip and the channel were modeled as two metal spheres separated by a dielectric. The spheres have radii of the radius of curvature of the tip and the FWHM of the charge response, respectively.

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