Strain-sensing cryogenic field-effect transistor for integrated strain detection in GaAs/AlGaAs microelectromechanical systems

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We have fabricated a strain-sensing cryogenic field-effect transistor (FET) from a GaAs/AlGaAs heterostructure containing a near-surface two-dimensional electron gas. The FET has transconductance 100 μS and a small signal drain-source resistance 10 MΩ. The charge noise has a flat spectrum at high frequencies with magnitude $0.2e/\sqrt{\text{Hz}}$ and $1/f$ noise corner less than 300 Hz. The piezoelectric effect couples stress in the substrate to the electron density in the FET channel giving an electrical response to applied strain. Strain sensitivity was measured to be $2\times10^{-9}/\sqrt{\text{Hz}}$, limited by FET noise. Integrated strain-sensing FETs offer advantages for detecting small forces in GaAs/AlGaAs microelectromechanical systems. © *1996 American Institute of Physics.* [S0003-6951(96)04226-X]

Micromachined GaAs systems provide a novel environment for studying new physical phenomena[1] and offer new possibilities for device applications.[2–4] When the size scale of these systems becomes small ($\approx$1 μm), the detection of mechanical deflection presents a challenge for displacement sensors. However, the strain produced by a force generally increases as the size of the mechanical structure is reduced. Thus, a strain-sensor presents an alternative to deflection sensors for detecting small forces in microelectromechanical systems (MEMS). Scanned probe microscope (SPM) cantilevers provide an important example of a small system where a strain sensor could be used. Currently most cantilevers rely on optical readouts of deflection which presents disadvantages if the sample being scanned is photosensitive. Alternative deflection sensing mechanisms have been developed including external readouts via capacitance[5] and integrated internal readouts via piezoresistive[6] and piezoelectric[7–9] cantilevers.

In this letter we describe the fabrication of a strain-sensing GaAs/AlGaAs field-effect transistor (FET) which can serve as an integrated strain sensor in MEMS. It is known that piezoelectric properties of GaAs affect FET parameters.[10–12] We exploit this dependence using low-noise FETs to make a strain sensor capable of detecting volume or dilatational strains $\epsilon < 2\times10^{-9}/\sqrt{\text{Hz}}$. Our FETs have a charge noise $q_n < 0.2e/\sqrt{\text{Hz}}$, where e is the charge of a single electron and a $1/f$ noise corner less than 300 Hz. As strain sensors these present several advantages: they can be made small (<1 μm), have a large operating bandwidth (>100 kHz), can be integrated directly into MEMS, and have low-power dissipation (<1 μW) which makes them suitable for operation at dilution refrigerator temperatures. Integrating these FETs into a SPM cantilever would allow operation with reduced cantilever size and increased sensitivity.

Our field-effect transistors are fabricated from a GaAs/AlGaAs heterostructure containing a near-surface two-dimensional electron gas (2DEG) using a design similar to Mar *et al.*[13] In our samples the two-dimensional electron gas with sheet density $n_S = 2\times10^{11}/\text{cm}^2$ and mobility $\mu = 1.5\times10^5$ cm^2/V s is confined by a 200 Å square well beginning 520 Å beneath the surface. Figure 1(a) shows a schematic of the FET geometry. The channel, defined using electron beam lithography and a mesa etch, has lithographic dimensions of 5 μm$\times$100 μm as indicated, and is U-shaped to anticipate fabrication on a SPM cantilever. The gate was made by thermally evaporating 200 Å of chrome followed by 2500 Å of gold over the channel giving a total gate area of 500 μm^2 and a nominal gate to channel capacitance of 1.0 pF. Electrical contact to the 2DEG was made by thermally diffusing AuNiGe contacts into the chip. The channel was current biased using a low-noise voltage source in series with a 1 MΩ resistor. Drain-source voltage was monitored with a PAR 113 preamplifier which has a noise temperature of less than 6.5 K for typical resistances (1 MΩ) and frequencies (10 Hz to 10 kHz) encountered in this experiment.

Figure 1(b) illustrates how strain was applied to the field-effect transistor. The chip 2.5 mm$\times$14 mm containing the FET was mounted on a piezoelectric bimorph which was driven through the resonant frequency of the chip. The FET

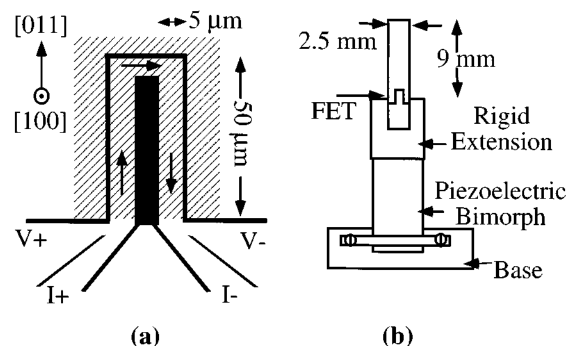

FIG. 1. (a) Schematic of field-effect transistor (FET) geometry. Dark lines are etch trenches, diagonal line pattern represents top gate, arrows indicate current path through channel. The [100] direction is out of the page and [011] is indicated. (b) Schematic of mounting system for FET substrate.

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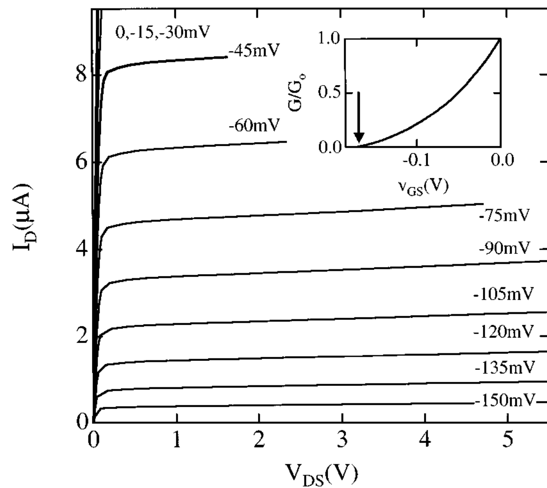

FIG. 2. Family of source-drain characteristics taken at $T \approx 10$ K. Voltages indicate gate-source voltage, V_{GS}. Inset shows a cutoff graph of channel conductance G normalized to its zero gate voltage value $G_0 = 2.5$ mS. The cutoff threshold ($V_T = -170$ mV) is indicated by the arrow.

was placed in the region of maximum strain near the clamped end of the chip as indicated. An aluminum piece reinforced with a small Macor block served as both a rigid extension to prevent the deformation of the bimorph from straining the sample and as a ground plane to isolate the sample from the relatively large voltages applied to the bimorph. The FET/bimorph assembly was mounted in vacuum inside a thermal shield attached to the cold plate of an Infrared Labs liquid helium Dewar with an opening in the shield to allow optical access to the entire chip. The sample temperature was ≈ 10 K due to heating from black body radiation through the optical access window located 7 cm away.

Figure 2 shows the measured drain characteristics for the field-effect transistor at $T \approx 10$ K. The transistor operates with low noise in the saturation region and displays a typical small-signal drain-source resistance $r_{ds} \approx 10$ MΩ and transconductance $g_m = 100$ μS which results in a transconductance per gate width of 20 mS/mm. No carrier heating effects were observed even when the depletion region was largest ($V_{GS} = -150$ mV and $V_{DS} = 6$ V) indicating that the electrons are strongly confined by the square well structure. The inset in Fig. 2 shows a plot of normalized channel conductance G versus gate voltage V_{GS}. The conductance changed by five orders of magnitude with V_{GS} from its zero gate voltage value $G_0 = 2.5$ mS. The small magnitude of the threshold voltage ($V_T = -170$ mV) gives excellent sensitivity while the smooth, constant curvature indicates little parallel conduction.

The measured gain and frequency response are in accord with simple field-effect transistor models. At a typical operating point ($V_{GS} = -85$ mV and $I_D = 3.8$ μA) the dimensionless voltage gain $A_v = 70$. Gain was found to vary with a square root dependence on drain current $A_v \propto I_D^{1/2}$ as expected.[14] A rolloff occurred above a 3 dB point of 400 Hz due to Dewar lead capacitance ≈ 400 pF. The ac output signal was constant up to 100 kHz for voltage biased measurements. A figure of merit for transistor speed is given by C_G / g_m, where C_G is the capacitance between the gate and the 2DEG. This indicates an intrinsic rolloff frequency of 16

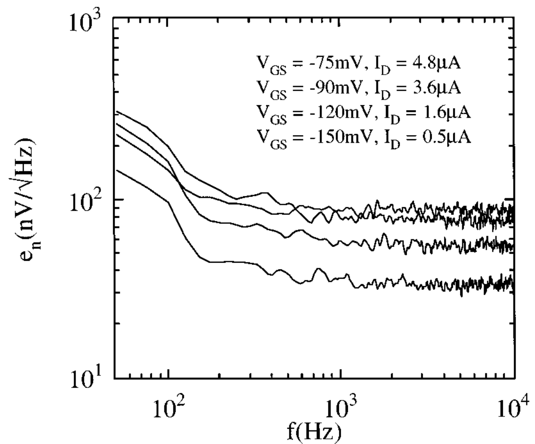

FIG. 3. Family of noise spectra taken at $T \approx 10$ K corrected for RC rolloff of the external circuit. The lowest white noise value corresponds to charge noise of $0.2e\sqrt{\text{Hz}}$. The $1/f$ noise corner is <300 Hz.

MHz for the geometry of Fig. 1(a). Much higher operating frequencies can be obtained using a FET with a shorter and wider channel.

Figure 3 shows measured spectra for voltage noise e_n referred to the input of the field-effect transistor. The noise is characterized by a flat spectrum at high frequencies with a low $1/f$ noise corner of 300 Hz. In the saturation region the magnitude of the noise e_n is independent of drain-source voltage V_{DS} for a given gate-source voltage V_{GS} but increases with increasing channel current as $e_n^2 \propto I_D$. The noise contribution from the external circuit is dominated by a white noise level of 20 nV/$\sqrt{\text{Hz}}$ from the voltage source used to apply a voltage to the gate; noise from the PAR 113 preamplifier is negligible. The lowest noise occurs for $V_{GS} = -150$ mV, where the charge noise $q_n = e_n C_G$ $< 0.2 \text{e}/\sqrt{\text{Hz}}$.

The field-effect transistor was subjected to strain by applying a variable frequency voltage ($0.25 V_{pp}$) to the bimorph to drive the chip through its lowest mechanical resonance. Figure 4(a) shows the measured small signal response v_{DS} of the FET for operating point $V_{GS} = -85$ mV and $I_D = 3.8$ μA

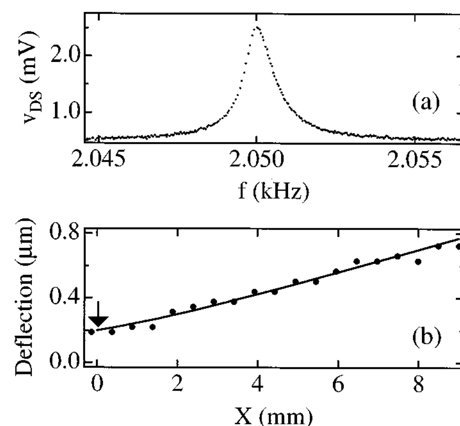

FIG. 4. (a) Small signal drain-source voltage v_{DS} for an operating point of $V_{GS} = -85$ mV and $I_D = 3.8$ μA as FET substrate is driven through its lowest mechanical resonance. (b) Measured deflection as a function of position along the length of the GaAs chip at its lowest mechanical resonance. Line indicates a fit to the data. The arrow denotes FET position.

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about the sharp ($Q=2000$) mechanical resonance of the chip. The strain at this resonance was measured using a Michelson interferometer operating through an optical access port in the Dewar. At $T\approx10$ K the resonating chip was placed at one arm of the interferometer. The resulting fringes were detected by a photodiode mounted behind a pinhole and recorded by a digital storage scope. By sliding the Dewar to expose different parts of the vibrating chip, data on amplitude of vibration as a function of position were obtained. Multiple measurements at each position on the chip were made and then averaged.

Figure 4(b) shows the amplitude of deflection along the entire length of the cantilever; the arrow indicates the position of the field-effect transistor. The data were fit to the equation of a driven cantilever beam[15] with boundary conditions of zero force and moment at the free end, fixed amplitude at the driven end and a slope at the driven end which was allowed to vary as a free parameter of the fit. The fit shown in Fig. 4(b) indicates a total volume strain ϵ in the FET region $\epsilon=7\times10^{-7}$. For this FET the normalized strain responsivity $r=N/A\epsilon$, where N is the change in number of gate electrons and A is the gate area, has a value $r=7.1\times10^{13}/\mathrm{cm}^2$. Combining this value with the measured charge noise gives a strain sensitivity of $\epsilon_n=2\times10^{-9}/\sqrt{\mathrm{Hz}}$. For comparison we consider a GaAs/AlGaAs SPM cantilever of typical dimensions (100 μm$\times$20 μm$\times$1 μm). With an integrated FET this cantilever would have force sensitivity <20 pN/$\sqrt{\mathrm{Hz}}$ and vertical resolution <0.5 Å/$\sqrt{\mathrm{Hz}}$. The maximum uniaxial strain $\epsilon_{\max}$ at the base of a cantilever with rectangular cross section is given by $\epsilon_{\max}=6Fl/(Et^2w)$,[15] where F is the force applied to the end of the cantilever, l, w, and t are the length, width, and thickness, respectively, and E is Young's modulus. The minimum vertical resolution is given by $u_{\min}=2\epsilon_{\mathrm{nu}}l^2/3t$, where ϵ_{nu} is the uniaxial strain sensitivity. These expressions show that force sensitivity and vertical resolution of a strain-sensing cantilevers increase for small sizes. Strain-sensing FETs can be made with submicron dimensions and low-power dissipation.

Two mechanisms which provide an electrical response to strain in GaAs are the piezoelectric effect[16] and the deformation potential.[17] Both couple strain to a change in the number of electrons in the FET channel. At the mechanical resonance peak we measure a change in amplitude of 250 gate electrons. The shift in the conduction band energy due to the deformation potential is given by $\Delta E_c=a\epsilon$,[18] where ΔE_c is the conduction band shift, $a=8$ eV is the hydrostatic pressure deformation potential, and ϵ is the volume strain. The shift in the number of gate electrons given by $\Delta N=C_G\Delta E_c/e^2$, where C_G is the gate/channel capacitance and e is the electronic charge results in 35 gate electrons shifting to equalize the chemical potential. The piezoelectric effect produces a polarization given by $P_i=d_{ijk}s_{jk}$,[16,19] where P_i is the induced polarization in the i direction, d_{ijk} is the piezoelectric tensor, and s_{jk} is the stress tensor. The stress given by the fit in Fig. 4(b) is applied in the [011] direction for the FET orientation with respect to the GaAs crystal axes indicated in Fig. 1(a). The resulting nominal polarization is perpendicular to the plane of the 2DEG and induces a change in amplitude of 740 electrons on the gate. Thus, the piezoelectric effect dominates the strain induced signal. The measured charge in our device is less than the maximum predicted for the piezoelectric effect.

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